INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8705F

Simple Low Pin Count Input / Output (Simple LPC I/O)

Preliminary Specification V0.3

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Revision History

Note: Words in bold typeface in the revisions below indicate the changes.

Section	Revision	Page No.
1	• The feature of Smart Card Reader was added. • The feature of "48 General Purpose I/O Pins" was revised.	1
2	• At the end of the second paragraph, the description "It also features a PC/SC and ISO 7816 compliant Smart Card Reader." was added.	3
3	• Block Diagram was revised.	5
4	• Section 4 Pin Configuration was revised.	7
	• Pin 2 was revised to "RTS2#/**JP6**". • Pin 11 was revised to "FD4/**IRQIN0**/GP14". • Pin 12 was revised to "FD5/**IRQIN1**/GP15". • Pin 13 was revised to "FD/**IRQIN2**/GP16". • Pin 14 was revised to "FD/**IRQIN3**/GP17". • Pin 16 was revised to "FA0/**VID_I0**/GP20". • Pin 17 was revised to "FA1/**VID_I1**/GP21". • Pin 18 was revised to "FA2/**VID_I2**/GP22". • Pin 19 was revised to "FA3/**VID_I3**/GP23". • Pin 20 was revised to "FA4/**VID_I4**/GP24". • Pin 21 was revised to "FA5/**VID_O1**/GP25". • Pin 22 was revised to "FA6/**VID_O2**/GP26". • Pin 23 was revised to "FA7/**VID_O3**/GP27". • Pin 24 was revised to "FA8/**VID_O4**/GP30". • Pin 25 was revised to "FA9/**VID_O5**/GP31". • Pin 47 was revised to "FCS#/**SCIO**/GP53". • Pin 59 was revised to "MTRB#/**SCRST**". • Pin 61 was revised to "DRVB#/**SCCLK**". • Pin 80 was revised to "FAN_CTL3/GP62/**SCPFET#**". • Pin 81 was revised to "PME#/GP63/**SCPRES#**".	8-9
5	• The pin descriptions of the revised pins described above were revised.	11-19
	• Add the note "The GPIO registers of these pins are powered by VCC, not VCCH." to the end of Table 5-4 and Table 5-5.	12-13
	• The pin descriptions of pins 69, 70, 71, 72 were revised.	17
6	• Section 6 List of GPIO Pins was revised.	21-23

Revision History (cont' d)

Section	Revision	Page No.
6	• Add the note "The GPIO registers of these pins are powered by VCC, not VCCH." to the end of Table 6-6.	23
7	• Table 7-1. Power On Strapping Options was revised.	25
8	• In Table 8-1, the register for index 22h was revised to "Configuration Select and Chip Version".	28
	• In Table 8-4, two more Serial Port Configuration registers were added: Serial Port 2 Special Configuration Register 3, and Serial Port 2 Special Configuration Register 4.	29
	• In Table 8-7, two more GPIO Configuration registers were added: IRQ Routing Input 0 and 1 Interrupt Level Select Register, and IRQ Routing Input 2 and 3 Interrupt Level Select Register.	31
	• Several new registers were added from Index F6h through FFh at the end of Table 8-7 GPIO Configuration Registers.	32
	• Section 8.3.5 Configuration Select and Chip Version Register was revised. • In section 8.3.6 Software Suspend, the bits 7-6 was revised to "SCRPRES# Select". • In section 8.3.7 Clock Selection and Flash ROM I/F Control Register, the description of bit 5 was revised to Flash ROM Interface Address Segment 2 (FFEF0000h-**F**FEFFFFh, FFEE0000h-FFEEFFFFh) Enable.	35
	• The bit 2-0 description for section 8.6.6 Serial Port 2 Special Register 2 was revised. It added the "100: Smart Card Reader (SCR).	44
	• The descriptions for Serial Port 2 Special Configuration Register 3 and Serial Port 2 Special Configuration Register 4 were added in section 8.6.7 and 8.6.8 respectively.	45
	• The bit 0 of section 8.8.9 PME Control Register 1 was revised to "Reserved".	49
	• Added 2 new registers in section 8.9.8, and 8.9.9: IRQ Routing Input 0 and 1 Interrupt Level Select Register, and IRQ Routing Input 2 and 3 Interrupt Level Select Register.	51
	• Added the descriptions of several new registers from section 8.9.20 through 8.9.29.	54-56
	• The descriptions of bits 7-6, 5-4, 3 of Section 8.12.5 MIDI Port Special Configuration Register were revised.	58
9	• In Table 9-2. Environment Controller Registers, the Serial Bus Interface Address Register was revised to "Reserved".	67

Revision History (cont' d)

Section	Revision	Page No.
9	• In Table 9-2. Environment Controller Registers, the registers from Index 52h to 54h were revised to "Reserved" registers. • In Table 9-2. Environment Controller Registers, 4 new EC registers were added from index 5Ch through 5Fh: 1) Special Control and Beep Event Enable Register, 2) Beep Frequency Divisor of Fan Event Register, 3) Beep Frequency Divisor of Voltage Event Register, and 4) Beep Frequency Divisor of Temperature Event Register.	68
	• The bit 6 description in section 9.5.3.2.11 Fan Tachometer Divisor Register was revised.	70
	• The R/W of section 9.5.3.2.13 Fan Tachometer 1-3 Limit Registers (Index=10h-12H) was revised to "**R/W**". • Bit 7 description of section 9.5.3.2.14 Fan Controller Main Control Register was revised. • Bits 7 & 6-4 descriptions of section 9.5.3.2.15 FAN_CTL Control Register were revised.	71
	• Section 9.5.3.2.26 Serial Bus Interface Address Register (Index=48h) was revised to "Reserved" register. • Section 9.5.3.2.28 bit no. 7 was revised to bit no. **7-6**.	73
	• The registers from Index 54h-52h was changed to "Reserved" registers in section 9.5.3.29.	74
	• In section 9.5.4.3 Voltage and Temperature Input, the formula for Negative Voltage was revised to "Vs = **(1+Rin/Rf) x Vin - (Rin/Rf) x VREF**".	78
	• The descriptions of the 4 new EC registers described above were given from section 9.5.3.2.32 through 9.5.3.2.35.	74-75
	• In section 9.7.2, the "DLAB=0" should be changed to "DLAB=**1**" in title (4) Divisor Latches (DLL, DLM).	111

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Timing Diagrams

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TABLES

1. Features

- **Low Pin Count Interface**
  - Compliant with Intel LPC Interface Specification Rev.1.0 (Sept. 29, 1997)
  - Supports Serial IRQ Protocol
  - Supports PCI PME# Interface

- **PC98/PC99, ACPI Compliant**
  - PC98 & PC99 compliant
  - Register sets compatible with "Plug and Play ISA Specification Rev. 1.0a"
  - ACPI V. 1.0 compliant
  - Supports 9 logical devices

- **Enhanced Hardware Monitor**
  - Built-in 8-bit Analog to Digital Converter
  - 3 thermal inputs from remote thermistors or thermal diode or diode-connected transistor
  - 8 voltage monitor inputs (VBAT is measured internally.)
  - Watch Dog comparison of all monitored values

- **Fan Speed Controller**
  - Provides Fan ON/OFF and PWM control
  - 3 programmable Pulse Width Modulation (PWM) Fan control outputs
  - Each PWM output supports 128 steps of PWM modes
  - Monitors 3 Fan tachometer inputs

- **Game Port**
  - Built-in 558 quad timers and buffer chips
  - Supports direct connection of two joysticks
  - Game port signals are multiplexed with GPIOs

- **Two 16C550 UARTs**
  - Supports two standard Serial ports
  - UART1 is dedicated for Serial port
  - UART2 supports either Serial Port or IrDA 1.0/ASKIR

- **MIDI Interface**
  - UART implementation
  - Supports direct connection to MPU-401 MIDI

- **Consumer Remote Control (TV remote) IR with Power-up Feature**

- **IEEE 1284 Parallel Port**
  - Standard mode -- Bi-directional SPP compliant
  - Enhanced mode -- EPP V.1.7 and 1.9 compliant
  - High speed mode -- ECP, IEEE 1284 compliant
  - Backdrive current reduction
  - Printer power-on damage reduction
  - Supports POST (Power-On Self Test) Data Port

- **Floppy Disk Controller**
  - Supports two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives
  - Enhanced digital data separator
  - 3-Mode drives supported
  - Supports automatic write protection via software

- **Smart Card Reader**
  - Compliant with Personal Computer Smart Card (PC/SC) Working Group standard
  - Compliant with smart card (ISO 7816) protocols
  - Supports card present detect
  - Supports one programmable clock frequency, 7.1 MHz, and 3.5 MHz (default) card clocks

- **48 General Purpose I/O Pins**
  - Input mode supports switch de-bounce
  - SMI is routed through GPIOs
  - Power LED Blinking Control
  - Hardware Monitor Warning Beep Output
  - External IRQ Inputs Routing into Serial IRQ
  - Watch Dog Timer

- **Flash ROM Interface**
  - Up to 4M bits flash supported

- **Single 24/48 MHz Clock Inputs**

- **Single +5V Power Supply**

- **128-Pin PQFP**

2. General Description

The IT8705F is a LPC Interface based highly integrated Super I/O. The IT8705F provides the most commonly used legacy Super I/O functionality plus the latest Environment Control initiatives, such as Hardware Monitor, Fan Speed Controller and ITE's "SmartGuardian" function. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.0" (Sept. 29, 1997). The IT8705F meets the "Microsoft® PC98 & PC99 System Design Guide" requirements and is ACPI compliant.

The IT8705F features the enhanced hardware monitor providing 3 thermal inputs from remote thermistors, thermal diode or diode-connected transistor (2N3904). The device also provides the ITE innovative intelligent automatic Fan ON/OFF & speed control functions (SmartGuardian) to reduce overall system noise and power consumption. It also features a PC/SC and ISO 7816 compliant Smart Card Reader.

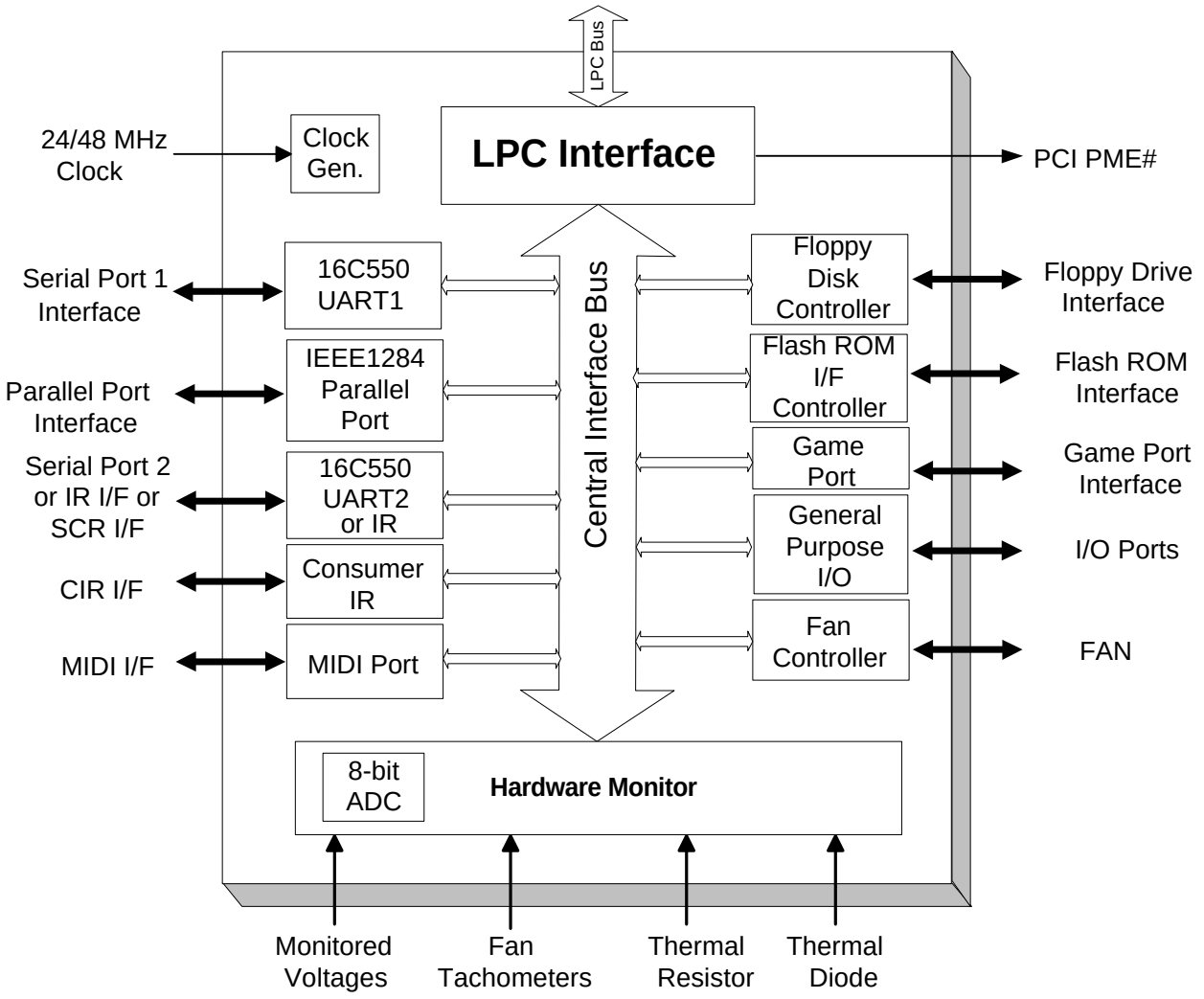
The IT8705F has integrated nine logical devices, featuring an Environment Controller (controls three Fans). The Environment Controller has temperature, voltage and Fan Speed monitors. One Fan Speed Controller is responsible to control three fan speeds through three 128 steps of Pulse Width Modulation (PWM) output pins and to monitor three fans' tachometer inputs.

Other features include one high-performance 2.88MB floppy disk controller, with digital data separator, supporting two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives. One multi-mode high-performance parallel port features the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9 are supported), and the IEEE 1284 compliant Extended Capabilities Port (ECP). Two 16C550 standard compatible enhanced UARTs perform asynchronous communication, and support SIR and one consumer remote control (TV remote) IR, one MPU-401 UART mode compatible MIDI port, one game port with built-in 558 quad timers and buffer chips to support direct connection of 2 joysticks, and six ports (48 GPIO pins). There is also a flash ROM interface with Address (FA[0:18]), Data (FD[0:7]), and supporting three control signals FCS#, FWE# and FRD#. In addition, a SmartGuardian engine is provided to monitor the system condition and reacts to the detected condition accordingly.

These nine logical devices can be individually enabled or disabled via software configuration registers. The IT8705F utilizes power-efficient circuitry to reduce power consumption. Once a logical device is disabled, the inputs are gated inhibit, the outputs are TRI-STATE and the input clock is disabled. The IT8705F requires a single 48/24 MHz clock input and operates with a single +5V power supply.

The IT8705F is available in 128-pin PQFP (Plastic Quad Flat Package).

3. Block Diagram



4. Pin Configuration

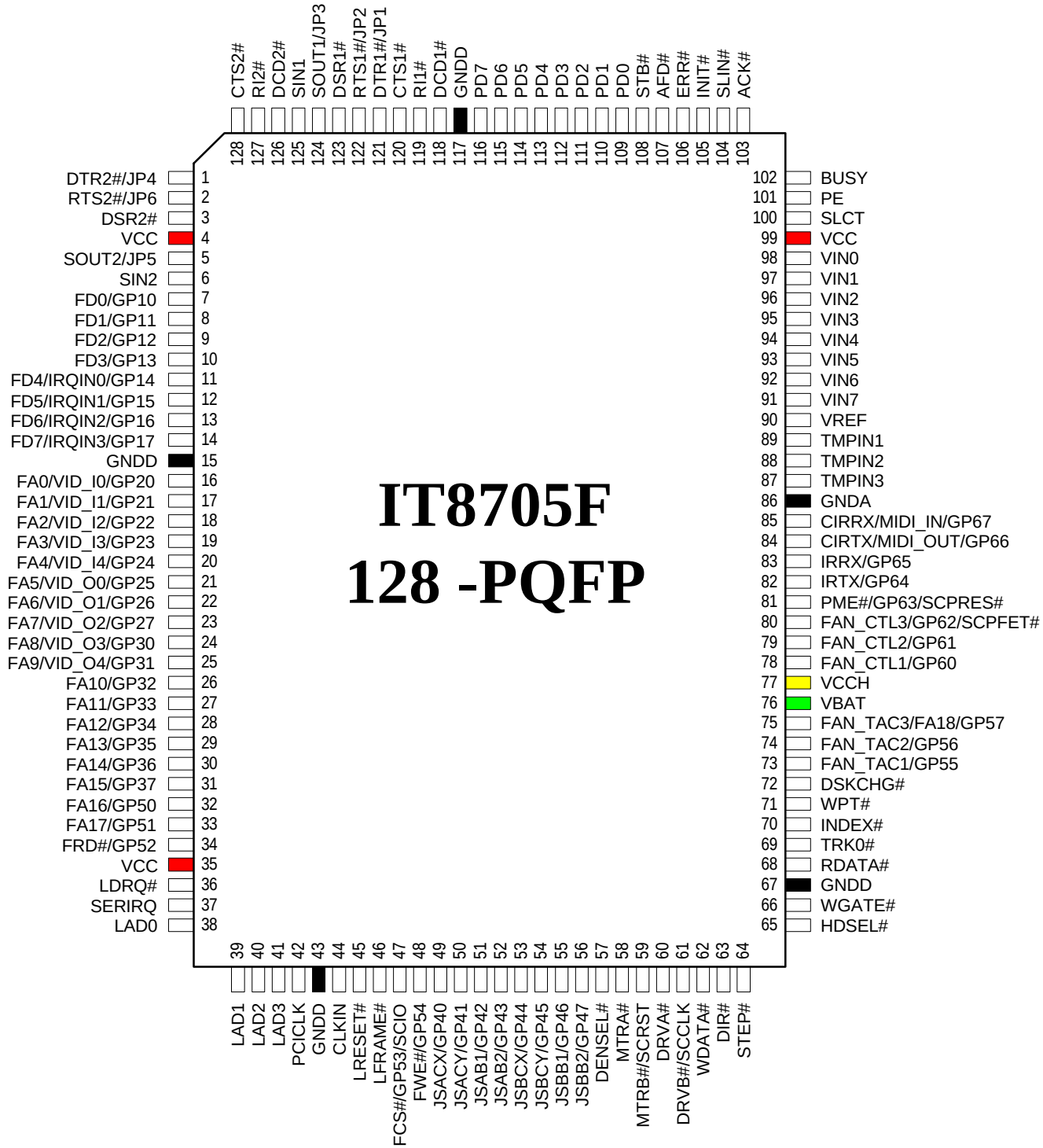


Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DTR2#/JP4	33	FA17/GP51	65	HDSEL#	97	VIN1
2	RTS2#/JP6	34	FRD#/GP52	66	WGATE#	98	VIN0
3	DSR2#	35	VCC	67	GNDD	99	VCC
4	VCC	36	LDRQ#	68	RDATA#	100	SLCT
5	SOUT2	37	SERIRQ	69	TRK0#	101	PE
6	SIN2	38	LAD0	70	INDEX#	102	BUSY
7	FD0/GP10	39	LAD1	71	WPT#	103	ACK#
8	FD1/GP11	40	LAD2	72	DSKCHG#	104	SLIN#
9	FD2/GP12	41	LAD3	73	FAN_TAC1/GP55	105	INIT#
10	FD3/GP13	42	PCICLK	74	FAN_TAC2/GP56	106	ERR#
11	FD4/IRQIN0/ GP14	43	GNDD	75	FAN_TAC3/FA18/ GP57	107	AFD#
12	FD5/IRQIN1/ GP15	44	CLKIN	76	VBAT	108	STB#
13	FD6/IRQIN2/ GP16	45	LRESET#	77	VCCH	109	PD0
14	FD7/IRQIN3/ GP17	46	LFRAME#	78	FAN_CTL1/GP60	110	PD1
15	GNDD	47	FCS#/SCIO/GP53	79	FAN_CTL2/GP61	111	PD2
16	FA0/VID_I0/GP20	48	FWE#/GP54	80	FAN_CTL3/GP62/ SCPFET#	112	PD3
17	FA1/VID_I1/GP21	49	JSACX/GP40	81	PME#/GP63/ SCPRES#	113	PD4
18	FA2/VID_I2/GP22	50	JSACY/GP41	82	IRTX/MIDI_OUT/ GP64	114	PD5
19	FA3/VID_I3/GP23	51	JSAB1/GP42	83	IRRX/MIDI_IN/ GP65	115	PD6
20	FA4/VID_I4/GP24	52	JSAB2/GP43	84	CIRTX/GP66	116	PD7
21	FA5/VID_O0/ GP25	53	JSBCX/GP44	85	CIRRX/GP67	117	GNDD
22	FA6/VID_O1/ GP26	54	JSBCY/GP45	86	GNDA	118	DCD1#
23	FA7/VID_O2/ GP27	55	JSBB1/GP46	87	TMPIN3	119	RI1#
24	FA8/VID_O3/ GP30	56	JSBB2/GP47	88	TMPIN2	120	CTS1#
25	FA9/VID_O4/ GP31	57	DENSEL#	89	TMPIN1	121	DTR1#/JP1
26	FA10/GP32	58	MTRA#	90	VREF	122	RTS1#/JP2
27	FA11/GP33	59	MTRB#/SCRST	91	VIN7	123	DSR1#
28	FA12/GP34	60	DRVA#	92	VIN6	124	SOUT1/JP3
29	FA13/GP35	61	DRVB#/SCCLK	93	VIN5	125	SIN1
30	FA14/GP36	62	WDATA#	94	VIN4	126	DCD2#
31	FA15/GP37	63	DIR#	95	VIN3	127	RI2#
32	FA16/GP50	64	STEP#	96	VIN2	128	CTS2#

Table 4-2. Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ACK#	103	FA4/VID_I4/GP24	20	IRTX/MIDI_OUT/ GP64	82	RTS1#/JP2	122
AFD#	107	FA5/VID_O0/ GP25	21	JSAB1/GP42	51	RTS2#/JP6	2
BUSY	102	FA6/VID_O1/ GP26	22	JSAB2/GP43	52	SERIRQ	37
CIRRX/GP67	85	FA7/VID_O2/ GP27	23	JSACX/GP40	49	SIN1	125
CIRTX/GP66	84	FA8/VID_O3/ GP30	24	JSACY/GP41	50	SIN2	6
CLKIN	44	FA9/VID_O4/ GP31	25	JSBB1/GP46	55	SLCT	100
CTS1#	120	FAN_CTL1/GP60	78	JSBB2/GP47	56	SLIN#	104
CTS2#	128	FAN_CTL2/GP61	79	JSBCX/GP44	53	SOUT1/JP3	124
DCD1#	118	FAN_CTL3/GP62/ SCPFET#	80	JSBCY/GP45	54	SOUT2	5
DCD2#	126	FAN_TAC1/GP55	73	LAD0	38	STB#	108
DENSEL#	57	FAN_TAC2/GP56	74	LAD1	39	STEP#	64
DIR#	63	FAN_TAC3/FA18/ GP57	75	LAD2	40	TMPIN1	89
DRVA#	60	FCS#/GP53/SCIO	47	LAD3	41	TMPIN2	88
DRVB#/SCCLK	61	FD0/GP10	7	LDRQ#	36	TMPIN3	87
DSKCHG#	72	FD1/GP11	8	LFRAME#	46	TRK0#	69
DSR1#	123	FD2/GP12	9	LRESET#	45	VBAT	76
DSR2#	3	FD3/GP13	10	MTRA#	58	VCC	4
DTR1#/JP1	121	FD4/GP14	11	MTRB#/SCRST	59	VCC	35
DTR2#/JP4	1	FD5/GP15	12	PCICLK	42	VCC	99
ERR#	106	FD6/GP16	13	PD0	109	VCCH	77
FA0/VID_I0/GP20	16	FD7/GP17	14	PD1	110	VIN0	98
FA1/VID_I1/GP21	17	FRD#/GP52	34	PD2	111	VIN1	97
FA10/GP32	26	FWE#/GP54	48	PD3	112	VIN2	96
FA11/GP33	27	GNDA	86	PD4	113	VIN3	95
FA12/GP34	28	GNDD	15	PD5	114	VIN4	94
FA13/GP35	29	GNDD	43	PD6	115	VIN5	93
FA14/GP36	30	GNDD	67	PD7	116	VIN6	92
FA15/GP37	31	GNDD	117	PE	101	VIN7	91
FA16/GP50	32	HDSEL#	65	PME#/GP63/ SCPRES#	81	VREF	90
FA17/GP51	33	INDEX#	70	RDATA#	68	WDATA#	62
FA2/VID_I2/GP22	18	INIT#	105	RI1#	119	WGATE#	66
FA3/VID_I3/GP23	19	IRRX/MIDI_IN/ GP65	83	RI2#	127	WPT#	71

5. IT8705F Pin Descriptions

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
4, 35, 99	**VCC**	PWR		***+5V Power Supply.***
76	**VBAT**	PWR		***+3.3V Battery Supply.***
77	**VCCH**	PWR		***+5V VCC Help Supply.***
15, 43, 67, 117	**GNDD**	GND		***Digital Ground.***
86	**GNDA**	GND		***Analog Ground.***

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
36	**LDRQ#**	DO16	VCC	***LPC DMA Request #.*** An encoded signal for DMA channel select.
37	**SERIRQ**	DIO16	VCC	***Serial IRQ.***
38 – 41	**LAD[0:3]**	DIO16	VCC	***LPC Address/Data 0-3.*** 4-bit LPC address / bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
42	**PCICLK**	DI	VCC	***LPC Clock.*** 33 MHz PCI Clock Input.
45	**LRESET#**	DI	VCC	***LPC RESET #.***
46	**LFRAME#**	DI	VCC	***LPC Frame #.*** This signal indicates the start of the LPC cycle.
81	**PME#/GP63/ SCPRES#**	DOD8/ DIOD8/ DI	VCCH	***Power Management Event # / General Purpose I/O 63. / Smart Card Present Detect #.*** • The first function of this pin is the power management event #, and supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from D3 (cold) state. This pin is backed by VCCH. • The second function of this pin is the General Purpose I/O Port 6 Bit 3. • The third function of this pin is Smart Card Present Detect #. This pin provides the Smart Card insertion detection for the Smart Card Reader interface. Upon detecting the insertion of the Smart Card, this pin will trigger the power-on event. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of Hardware Monitor Signals [Note1]

Pin(s) No.	Symbol	Attribute	Power	Description
98 – 91	**VIN[0:7]**	AI	VCC	***Voltage Analog Inputs [0:7].*** 0 to 4.096V FSR Analog Inputs.
90	**VREF**	AO	VCC	***Reference Voltage Output.*** Regulated referenced voltage for 3 external temperature sensors and negative voltage monitor.
89 – 87	**TMPIN[1:3]**	AI	VCC	***External Thermal Inputs [1:3].*** Connected to thermistor [1:3] or thermal diode [1:3].
73 – 74	**FAN_TAC [1:2]/ GP5[5:6]**	DI/ DIOD8	VCC	***Fan Tachometer Inputs [1:2]*** / ***General Purpose I/O 5[5:6].*** • The first functions of these pins are Fan tachometer inputs [1:2]. (0 to +5V amplitude fan tachometer input) • The second functions of these pins are General Purpose I/O Port 5 Bits 5-6. • The function configurations of these pins are determined by programming the software configuration registers.

Table 5-3. Pin Description of Hardware Monitor Signals [Note1] [cont'd]

Pin(s) No.	Symbol	Attribute	Power	Description
75	**FAN_TAC3/ FA18/ GP57**	DI/ DO/ DIOD8	VCC	***Fan Tachometer Inputs 3 / Flash ROM Interface Address 18 / General Purpose I/O 57.*** • The first function of this pin is Fan Tachometer Inputs 3 (0 to +5V amplitude fan tachometer input). • The second function of this pin is the Flash ROM Interface Address 18. • The third function of this pin is General Purpose I/O Port 5 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-4. Pin Description of Fan Controller Signals [Note]

Pin(s) No.	Symbol	Attribute	Power	Description
78 – 79	**FAN_CTL [1:2]/ GP6[0:1]**	DOD8/ DIOD8	VCCH	***FAN Control Outputs [1:2] / General Purpose I/O 6[0:1].*** • The first functions of these pins are Fan Control Outputs [1:2]. (PWM output signal to Fan's FET.) • The second functions of these pins are General Purpose I/O Port 6 Bits 0-1. • The function configurations of these pins are determined by programming the software configuration registers.
80	**FAN_CTL3/ GP62/ SCPFET#**	DOD8/ DIOD8/ DOD8	VCCH	***FAN Control Output 3 / General Purpose I/O 62 / Smart Card Power FET Control Output#.*** • The first functions of these pins are Fan Control Outputs [1:3]. (PWM output signal to Fan's FET.) • The second functions of these pins are General Purpose I/O Port 6 Bits 0-2. • The third function of this pin is Smart Card Power FET Control Output #. The Smart Card Reader interface requires this pin to drive an external Power FET to supply the current for the Smart Card (65 mA typical, 100 mA short to ground). • The function configurations of these pins are determined by programming the software configuration registers.

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 5-5. Pin Description of Infrared Port Signals [Note]

Pin(s) No.	Symbol	Attribute	Power	Description
82	**IRTX/GP64**	DO8/ DIOD8	VCCH	***Infrared Transmit Output / General Purpose I/O 64.*** • The first function of this pin is the Infrared Transmit Output. • The second function of this pin is the General Purpose I/O Port 6 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.
83	**IRRX/GP65**	DI/ DIOD8	VCCH	***Infrared Receive Input / General Purpose I/O 65.*** • The first function of this pin is the Infrared Receive Input. • The second function of this pin is the General Purpose I/O Port 6 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-5. Pin Description of Infrared Port Signals (cont'd)

Pin(s) No.	Symbol	Attribute	Power	Description
84	**CIRTX/ MIDI_OUT/ GP66**	DO8/ DO8/ DIOD8	VCCH	***Consumer Infrared Transmit Output / MIDI Output / General Purpose I/O 66.*** • The first function of this pin is the Consumer Infrared Transmit Output. • The second function of this pin is the MIDI Output. • The third function of this pin is the General Purpose I/O Port 6 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.
85	**CIRRX/ MIDI_IN/ GP67**	DI/ DI/ DIOD8	VCCH	***Consumer Infrared Receive Input / MIDI Input / General Purpose I/O 67.*** • The first function of this pin is the Consumer Infrared Receive Input. • The second function of this pin is the MIDI Input. • The third function of this pin is the General Purpose I/O Port 6 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 5-6. Pin Description of Game Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
49	**JSACX/ GP40**	DIOD8/ DIOD8	VCC	***Joystick A Coordinate X / General Purpose I/O 40.*** • The first function of this pin is the joystick A Coordinate X. • The second function of this pin is the General Purpose I/O Port 4 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.
50	**JSACY/ GP41**	DIOD8/ DIOD8	VCC	***Joystick A Coordinate Y / General Purpose I/O 41.*** • The first function of this pin is the joystick A Coordinate Y. • The second function of this pin is the General Purpose I/O Port 4 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
51	**JSAB1/ GP42**	DI/ DIOD8	VCC	***Joystick A Button 1 / General Purpose I/O 42.*** • The first function of this pin is the joystick A Button 1. • The second function of this pin is the General Purpose I/O Port 4 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
52	**JSAB2/ GP43**	DI/ DIOD8	VCC	***Joystick A Button 2 / General Purpose I/O 43.*** • The first function of this pin is the joystick A Button 2. • The second function of this pin is the General Purpose I/O Port 4 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
53	**JSBCX/ GP44**	DIOD8/ DIOD8	VCC	***Joystick B Coordinate X / General Purpose I/O 44.*** • The first function of this pin is the joystick B Coordinate X. • The second function of this pin is the General Purpose I/O Port 4 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-6. Pin Description of Game Port Signals (cont' d)

Pin(s) No.	Symbol	Attribute	Power	Description
54	**JSBCY/ GP45**	DIOD8/ DIOD8	VCC	***Joystick B Coordinate Y / General Purpose I/O 45.*** • The first function of this pin is the joystick B Coordinate Y. • The second function of this pin is the General Purpose I/O Port 4 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
55	**JSBB1/ GP46**	DI/ DIOD8	VCC	***Joystick B Button 1 / General Purpose I/O 46.*** • The first function of this pin is the joystick B Button 1 Input. • The second function of this pin is the General Purpose I/O Port 4 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.
56	**JSBB2/ GP47**	DI/ DIOD8	VCC	***Joystick B Button 2 / General Purpose I/O 47.*** • The first function of this pin is the joystick B Button 2 Input. • The second function of this pin is the General Purpose I/O Port 4 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-7. Pin Description of Serial Port 1 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
118	**DCD1#**	DI	VCC	***Data Carrier Detect 1 #.*** When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
119	**RI1#**	DI	VCC	***Ring Indicator 1 #.*** When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
120	**CTS1#**	DI	VCC	***Clear to Send 1 #.*** When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
121	**DTR1#/JP1**	DO8/DI	VCC	***Data Terminal Ready 1 # / JP1.*** When the signal is low, this output indicates to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. During LRESET#, this pin is input for JP1 power-on strapping option.
122	**RTS1#/JP2**	DO8/DI	VCC	***Request to Send 1 # / JP2.*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. During LRESET#, this pin is input for JP2 power-on strapping option.
123	**DSR1#**	DI	VCC	***Data Set Ready 1 #.*** When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-7. Pin Description of Serial Port 1 Signals (cont' d)

Pin(s) No.	Symbol	Attribute	Power	Description
124	**SOUT1/JP3**	DO8/DI	VCC	***Serial Data Out 1 / JP3.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation. During LRESET#, this pin is input for JP3 power-on strapping option.
125	**SIN1**	DI	VCC	***Serial Data In 1.*** This input receives serial data from the communications link.

Table 5-8. Pin Description of Serial Port 2 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
126	**DCD2#**	DI	VCC	***Data Carrier Detect 2 #.*** When this signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
127	**RI2#**	DI	VCC	***Ring Indicator 2 #.*** When this signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI signal is a MODEM status input whose condition can be tested by reading the MSR register.
128	**CTS2#**	DI	VCC	***Clear to Send 2 #.*** When this signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
1	**DTR2#/JP4**	DO8/DI	VCC	***Data Terminal ready 2 # / JP4.*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. *During LRESET#, this pin is input for JP4 power-on strapping option.*
2	**RTS2#/JP6**	DO8/DI	VCC	***Request to Send 2 # / JP6.*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. *During LRESET#, this pin is input for JP6 power-on strapping option.*
3	**DSR2#**	DI	VCC	***Data Set Ready 2 #.*** When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
5	**SOUT2/JP5**	DO8/DI	VCC	***Serial Data Out 2 / JP5.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. *During LRESET#, this pin is input for JP5 power-on strapping option.*
6	**SIN2**	DI	VCC	***Serial Data In 2.*** This input receives serial data from the communications link.

Table 5-9. Pin Description of Parallel Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
100	**SLCT**	DI	VCC	***Printer Select.*** This signal goes high when the line printer has been selected.
101	**PE**	DI	VCC	***Printer Paper End.*** This signal is set high by the printer when it runs out of paper.
102	**BUSY**	DI	VCC	***Printer Busy.*** This signal goes high when the line printer has a local operation in progress and cannot accept data.
103	**ACK#**	DI	VCC	***Printer Acknowledge #.*** This signal goes low to indicate that the printer has already received a character and is ready to accept another.
104	**SLIN#**	DIO24	VCC	***Printer Select Input #.*** When this signal is low, the printer is selected. This signal is derived from the complement of the bit 3 of the printer control register.
105	**INIT#**	DIO24	VCC	***Printer Initialize #.*** When this signal is active low, this signal is derived from the bit 2 of the printer control register, and is used to initialize the printer.
106	**ERR#**	DI	VCC	***Printer Error #.*** When this signal is active low, it indicates that the printer has encountered an error. The error message can be read from the bit 3 of the printer status register.
107	**AFD#**	DIO24	VCC	***Printer Auto Line Feed #.*** This signal is active low, and is derived from the complement of the bit 1 of the printer control register, and is used to advance one line after each line is printed.
108	**STB#**	DIO24	VCC	***Printer Strobe #.*** This signal is active low, and is derived from the complement of the bit 0 of the printer control register, and is used to strobe the printing data into the printer.
109 – 116	**PD[0:7]**	DIO24	VCC	***Parallel Port Data Bus 0-7.*** This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is de-selected.

Table 5-10. Pin Description of Floppy Disk Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
57	**DENSEL#**	DO40	VCC	***FDD Density Select #.*** DENSEL# is high for high data rates (500 Kbps, 1 Mbps). DENSEL# is low for low data rates (250 Kbps, 300 Kbps).
58	**MTRA#**	DO40	VCC	***FDD Motor A Enable #.*** Active low.
59	**MTRB#/ SCRST**	DO40/ DOD40	VCC	***FDD Motor B Enable #. / Smart Card Reset.*** • The first function of this pin is FDD Motor B Enable #. • The second function of this pin is Smart Card Reset. • The function configuration of this pin is decided by the software configuration registers.
60	**DRVA#**	DO40	VCC	***FDD Drive A Enable #.*** Active low.
61	**DRVB#/ SCCLK**	DO40/ DOD40	VCC	***FDD Drive B Enable # / Smart Card Clock.*** • The first function of this pin is the FDD Drive B Enable #. • The second function of this pin is Smart Card Clock. Three different card clocks are selectable from this pin: high speed (7.1 MHz), low speed (Default: 3.5 MHz) and a programmable card clock. • The function configuration of this pin is determined by the software configuration registers.
62	**WDATA#**	DO40	VCC	***FDD Write Serial Data to the Drive #.*** Active low.
63	**DIR#**	DO40	VCC	***FDD Head Direction #.*** This output determines the direction the FDC head movement during the SEEK operation. When the output is high, the head will step in. Otherwise, the head will step out.
64	**STEP#**	DO40	VCC	***FDD Step Pulse #.*** Active low.
65	**HDSEL#**	DO40	VCC	***FDD Head Select #.*** Active low.
66	**WGATE#**	DO40	VCC	***FDD Write Gate Enable #.*** Active low.
68	**RDATA#**	DI	VCC	***FDD Read Disk Data #.*** Active low. Serial data input from the FDD.
69	**TRK0#**	DI	VCC	***FDD Track 0 #.*** Active low. Indicates that the head of the selected drive is on track 0.
70	**INDEX#**	DI	VCC	***FDD Index #.*** Active low. Indicates the beginning of a disk track.
71	**WPT#**	DI	VCC	***FDD Write Protect #.*** Active low. Indicates that the disk of the selected drive is write-protected.
72	**DSKCHG#**	DI	VCC	***Floppy Disk Change #.*** Active low. This is an input pin that senses whether the drive door has been opened or a diskette has been changed.

Table 5-11. Pin Description of Flash ROM Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
7 – 10	**FD[0:3]/ GP1[0:3]**	DO8/ DIOD8	VCC	***Flash ROM Interface Data [0:3]/ General Purpose I/O 1[0:3].*** • The first functions of these pins are the Flash ROM interface Data [0:3]. • The second functions of these pins are the General Purpose I/O Port 1 Bits 0-3. • The function configurations of these pins are determined by programming the software configuration registers.
11 – 14	**FD[4:7]/ GP1[4:7]/ IRQIN[0:3]**	DO8/ DIOD8/ DI	VCC	***Flash ROM Interface Data [4:7]/ General Purpose I/O 1[4:7] /Interrupt Request Routing Input [0: 3].*** • The first functions of these pins are the Flash ROM interface Data [4:7]. • The second functions of these pins are the General Purpose I/O Port 1 Bits 4-7. • The third functions of these pins are the Interrupt Request Routing Input [0:3]. • The function configurations of these pins are determined by programming the software configuration registers.
16 – 20	**FA[0:4]/ GP2[0:4]/ VID_I[0:4]**	DO8/ DIOD8/ DI	VCC	***Flash ROM Interface Address[0:4] / General Purpose I/O 2[0:4] / Voltage ID Input [0:4].*** • The first functions of these pins are the Flash ROM Interface Address [0:4]. • The second functions of these pins are the General Purpose I/O Port 2 Bits 0-4. • The third functions of these pins are the Voltage ID Input [0:4]. • The function configurations of these pins are determined by programming the software configuration registers.
21 – 23	**FA[5:7]/ GP2[5:7]/ VID_O[0:2]**	DO8/ DIOD8/ DO8	VCC	***Flash ROM Interface Address[5:7] / General Purpose I/O 2[5:7] / Voltage ID Output [0:2].*** • The first functions of these pins are the Flash ROM Interface Address [5:7]. • The second functions of these pins are the General Purpose I/O Port 2 Bits 5-7. • The third functions of these pins are the Voltage ID Output [0:2]. • The function configurations of these pins are determined by programming the software configuration registers.
24 – 25	**FA[8:9]/ GP3[0:1]/ VID_O[3:4]**	DO8/ DIOD8/ DO8	VCC	***Flash ROM Interface Address[8:9] / General Purpose I/O 3[0:1] / Voltage ID Output [3:4].*** • The first functions of these pins are the Flash ROM Interface Address [8:9]. • The second functions of these pins are the General Purpose I/O Port 3 Bits 0-1. • The third functions of these pins are the Voltage ID Output [3:4]. • The function configuration of this pin is determined by programming the software configuration registers.
26 – 31	**FA[10:15]/ GP3[2:7]**	DO8/ DIOD8	VCC	***Flash ROM Interface Address[10:15] / General Purpose I/O 3[2:7].*** • The first functions of these pins are the Flash ROM Interface Address [10:15]. • The second functions of these pins are the General Purpose I/O Port 3 Bits 2-7. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-11. Pin Description of Flash ROM Interface Signals (cont'd)

Pin(s) No.	Symbol	Attribute	Power	Description
32 – 33	**FA[16:17]/ GP5[0:1]**	DO8/ DIOD8	VCC	***Flash ROM Interface Address[16:17]/ General Purpose I/O 5[0:1].*** • The first function of these pins is Flash ROM Interface address [16:17]. • The second function of these pins is General Purpose I/O Port 5 Bits 0-1. • The function configurations of these pins are determined by programming the software configuration registers.
34	**FRD#/GP52**	DO8/ DIOD8	VCC	***Flash ROM Interface Read Strobe # / General Purpose I/O 52.*** • The first function of this pin is the Flash ROM Interface Read Strobe#. • The second function of this pin is the General Purpose I/O Port 5 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
47	**FCS#/GP53/ SCIO**	DO8/ DIOD8/ DIOD8	VCC	***Flash ROM Interface Chip Select # / General Purpose I/O 53 / Smart Card Serial Data I/O.*** • The first function of this pin is the Flash ROM Interface Chip Select #. • The second function of this pin is the General Purpose I/O Port 5 Bit 3. • The third function of this pin is Smart Card Serial Data I/O. • The function configuration of this pin is determined by programming the software configuration registers.
48	**FWE#/GP54**	DO8/ DIOD8	VCC	***Flash ROM Interface Write Enable #/ General Purpose I/O 54.*** • The first function of this pin is the Flash ROM Interface Write Enable #. • The second function of this pin is the General Purpose I/O Port 5 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-12. Pin Description of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
44	**CLKIN**	DI	VCC	***24 MHz or 48 MHz Clock Input.***

IO Cell:

DO: Digital Output
DO8: 8mA Digital output buffer
DO16: 16mA Digital output buffer
DO40: 48mA Digital output buffer
DOD40: 48mA Digital Open-Drain output buffer

DIOD8: 8mA Digital Open-Drain Input/Output buffer

DIO8: 8mA Digital Input/Output buffer
DIO24: 24mA Digital Input/Output buffer

DI: Digital Input
AI: Analog Input
AO: Analog Output

Note 1: In addition to providing a highly integrated chip, ITE has also implemented a "SmartGuardian Utility" for hardware monitor application, providing a total solution for customers. The "SmartGuardian Utility" and the application circuit of hardware monitor function (the function arrangement of VIN0-7, TMPIN1-3, FAN_TAC1-3 and FAN_CTL1-3) are interdependent; that is, the " Smart Guardian Utility" is programmed according to the application circuit of hardware monitor function. ITE strongly recommends customers to follow the referenced application circuit of IT8705F to reduce the "time-to-market" schedule.

Pin No.	Symbol	Recommended Function Arrangement
98	VIN0	2 Volt for VCORE1 of CPU.
97	VIN1	2 Volt for VCORE2 of CPU.
96	VIN2	3.3 Volt for system.
95	VIN3	5 Volt for system.
94	VIN4	+12 Volt for system.
93	VIN5	-12 Volt for system.
92	VIN6	-5 Volt for system.
91	VIN7	5 Volt for Standby power.

6. List of GPIO Pins

Table 6-1. General Purpose I/O Group 1

Symbol	Pin #	Attribute	Description
FD0/GP10	**7**	DO8/ DIOD8	***Flash ROM Interface Data 0 / General Purpose I/O Port 1 Bit 0.***
FD1/GP11	**8**	DO8/ DIOD8	***Flash ROM Interface Data 1 / General Purpose I/O Port 1 Bit 1.***
FD2/GP12	**9**	DO8/ DIOD8	***Flash ROM Interface Data 2 / General Purpose I/O Port 1 Bit 2.***
FD3/GP13	**10**	DO8/ DIOD8	***Flash ROM Interface Data 3 / General Purpose I/O Port 1 Bit 3.***
FD4/IRQIN0/ GP14	**11**	DO8/DI/ DIOD8	***Flash ROM Interface Data 4 / Interrupt Request Routing Input 0 / General Purpose I/O Port 1 Bit 4.***
FD5/IRQIN1/ GP15	**12**	DO8/DI/ DIOD8	***Flash ROM Interface Data 5 / Interrupt Request Routing Input 1 / General Purpose I/O Port 1 Bit 5.***
FD6/IRQIN2/ GP16	**13**	DO8/DI/ DIOD8	***Flash ROM Interface Data 6 / Interrupt Request Routing Input 2 / General Purpose I/O Port 1 Bit 6.***
FD7/IRQIN3/ GP17	**14**	DO8/DI/ DIOD8	***Flash ROM Interface Data 7 / Interrupt Request Routing Input 3 / General Purpose I/O Port 1 Bit 7.***

Table 6-2. General Purpose I/O Group 2

Symbol	Pin #	Attribute	Description
FA0/GP20/ VID_I0	**16**	DO8/ DIOD8/DI	***Flash ROM Interface Address 0 / General Purpose I/O Port 2 Bit 0 / Voltage ID Input 0.***
FA1/GP21 /VID_I1	**17**	DO8/ DIOD8/DI	***Flash ROM Interface Address 1 / General Purpose I/O Port 2 Bit 1 / Voltage ID Input 1.***
FA2/GP22/ VID_I2	**18**	DO8/ DIOD8/DI	***Flash ROM Interface Address 2 / General Purpose I/O Port 2 Bit 2 / Voltage ID Input 2.***
FA3GP23/ VID_I3	**19**	DO8/ DIOD8/DI	***Flash ROM Interface Address 3 / General Purpose I/O Port 2 Bit 3 / Voltage ID Input 3.***
FA4/GP24/ VID_I4	**20**	DO8/ DIOD8/DI	***Flash ROM Interface Address 4 / General Purpose I/O Port 2 Bit 4 / Voltage ID Input 4.***
FA5/GP25/ VID_O0	**21**	DO8/ DIOD8/DO	***Flash ROM Interface Address 5 / General Purpose I/O Port 2 Bit 5 / Voltage ID Output 0.***
FA6/GP26/ VID_O1	**22**	DO8/ DIOD8/DO	***Flash ROM Interface Address 6 / General Purpose I/O Port 2 Bit 6 / Voltage ID Output 1.***
FA7/GP27/ VID_O2	**23**	DO8/ DIOD8/DO	***Flash ROM Interface Address 7 / General Purpose I/O Port 2 Bit 7 / Voltage ID Output 2.***

Table 6-3. General Purpose I/O Group 3

Symbol	Pin #	Attribute	Description
FA8/GPIO30 /VID_O3	**24**	DO8/ DIOD8/DO	***Flash ROM Interface Address 8 / General Purpose I/O Port 3 Bit 0 / Voltage ID Output 3.***
FA9/GPIO31 /VID_O4	**25**	DO8/ DIOD8/DO	***Flash ROM Interface Address 9 / General Purpose I/O Port 3 Bit 1 / Voltage ID Output 4.***
FA10/ GPIO32	**26**	DO8/ DIOD8	***Flash ROM Interface Address 10 / General Purpose I/O Port 3 Bit 2.***
FA11/ GPIO33	**27**	DO8/ DIOD8	***Flash ROM Interface Address 11 / General Purpose I/O Port 3 Bit 3.***
FA12/ GPIO34	**28**	DO8/ DIOD8	***Flash ROM Interface Address 12 / General Purpose I/O Port 3 Bit 4.***
FA13/ GPIO35	**29**	DO8/ DIOD8	***Flash ROM Interface Address 13 / General Purpose I/O Port 3 Bit 5.***
FA14/ GPIO36	**30**	DO8/ DIOD8	***Flash ROM Interface Address 14 / General Purpose I/O Port 3 Bit 6.***
FA15/ GPIO37	**31**	DO8/ DIOD8	***Flash ROM Interface Address 15 / General Purpose I/O Port 3 Bit 7.***

Table 6-4. General Purpose I/O Group 4

Symbol	Pin #	Attribute	Description
JSACX/ GP40	**49**	DIOD8/ DIOD8	***Joystick A Coordinate X / General Purpose I/O Port 4 Bit 0.***
JSACY/ GP41	**50**	DIOD8/ DIOD8	***Joystick A Coordinate Y / General Purpose I/O Port 4 Bit 1.***
JSAB1/ GP42	**51**	DI/ DIOD8	***Joystick A Button 1 / General Purpose I/O Port 4 Bit 2.***
JSAB2/ GP43	**52**	DI/ DIOD8	***Joystick A Button 2 / General Purpose I/O Port 4 Bit 3.***
JSBCX/ GP44	**53**	DIOD8/ DIOD8	***Joystick B Coordinate X / General Purpose I/O Port 4 Bit 4.***
JSBCY/ GP45	**54**	DIOD8/ DIOD8	***Joystick B Coordinate Y / General Purpose I/O Port 4 Bit 5.***
JSBB1/ GP46	**55**	DI/ DIOD8	***Joystick B Button 1 / General Purpose I/O Port 4 Bit 6.***
JSBB2/ GP47	**56**	DI/ DIOD8	***Joystick B Button 2 / General Purpose I/O Port 4 Bit 7.***

Table 6-5. General Purpose I/O Group 5

Symbol	Pin #	Attribute	Description
FA16/ GP50	**32**	DO8/ DIOD8	***Flash ROM Interface Address 16 / General Purpose I/O Port 5 Bit 0.***
FA17/ GP51	**33**	DO8/ DIOD8	***Flash ROM Interface Address 17 / General Purpose I/O Port 5 Bit 1.***
FRD#/ GP52	**34**	DO8/ DIOD8	***Flash ROM Interface Read Strobe # / General Purpose I/O Port 5 Bit 2.***
FCS#/ GP53/ SCIO	**47**	DO8/DIOD 8/DIOD8	***Flash ROM Interface Chip Select # / General Purpose I/O Port 5 Bit 3 / Smart Card Serial Data I/O.***
FWE#/ GP54	**48**	DO8/ DIOD8	***Flash ROM Interface Write Enable # / General Purpose I/O Port 5 Bit 4.***
FAN_TAC1/ GP55	**73**	DI/ DIOD8	***Fan Tachometer Input 1 / General Purpose I/O Port 5 Bit 5.***
FAN_TAC2/ GP56	**74**	DI/ DIOD8	***Fan Tachometer Input 2 / General Purpose I/O Port 5 Bit 6.***
FAN_TAC3/ FA18/GP57	**75**	DI/DO8/ DIOD8	***Fan Tachometer Input 3 / Flash ROM Interface Address 18 / General Purpose I/O Port 5 Bit 7.***

Table 6-6. General Purpose I/O Group 6[Note]

Symbol	Pin #	Attribute	Description
FAN_CTL1/ GP60	**78**	DOD8/ DIOD8	***Fan Control Output 1 / General Purpose I/O Port 6 Bit 0.***
FAN_CTL2/ GP61	**79**	DOD8/ DIOD8	***Fan Control Output 2 / General Purpose I/O Port 6 Bit 1.***
FAN_CTL3/ GP62/ SCPFET#	**80**	DOD8/ DIOD8/ DOD8	***Fan Control Output 3 / General Purpose I/O Port 6 Bit 2 / Smart Card Power FET Control Output#.***
PME#/GP63/ SCPRES#	**81**	DOD8/ DIOD8/DI	***Power Management Event # / General Purpose I/O Port 6 Bit 3 / Smart Card Present Detect#.***
IRTX/GP64	**82**	DO8/ DIOD8	***Infrared Transmit Output / General Purpose I/O Port 6 Bit 4.***
IRRX/GP65	**83**	DI/ DIOD8	***Infrared Receive Input / General Purpose I/O Port 6 Bit 5.***
CIRTX/ MIDI_OUT/ GP66	**84**	DO8/ DO8/ DIOD8	***Consumer Infrared Transmit Output / MIDI Output / General Purpose I/O Port 6 Bit 6.***
CIRRX/ MIDI_IN/ GP67	**85**	DI/DI/ DIOD8	***Consumer Infrared Receive Input / MIDI Input / General Purpose I/O Port 6 Bit 7.***

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 6-7. Programming of Pins 82, 83, 84, and 85

Programming Condition			Pin 82
All, 2Ah, Bit 4	**LDN4, F4h, Bit 6**	**LDN7, F0h, Bit 5**	
1	X	X	GP64
0	0	X	IRTX
0	1	0	IRTX
0	1	1	CIRTX

Programming Condition		Pin 83
All, 2Ah, Bit 5	**LDN4, F4h, Bit 6**	
1	X	GP65
0	0	IRRX
0	1	IRRX/CIRRX

Programming Condition		Pin 84
All, 2Ah, Bit 6	**LDN4, F4h, Bit 6**	
1	X	GP66
0	0	CIRTX
0	1	MIDI_OUT

Programming Condition		Pin 85
All, 2Ah, Bit 7	**LDN4, F4h, Bit 6**	
1	X	GP67
0	0	CIRRX
0	1	MIDI_IN

7. Power On Strapping Options

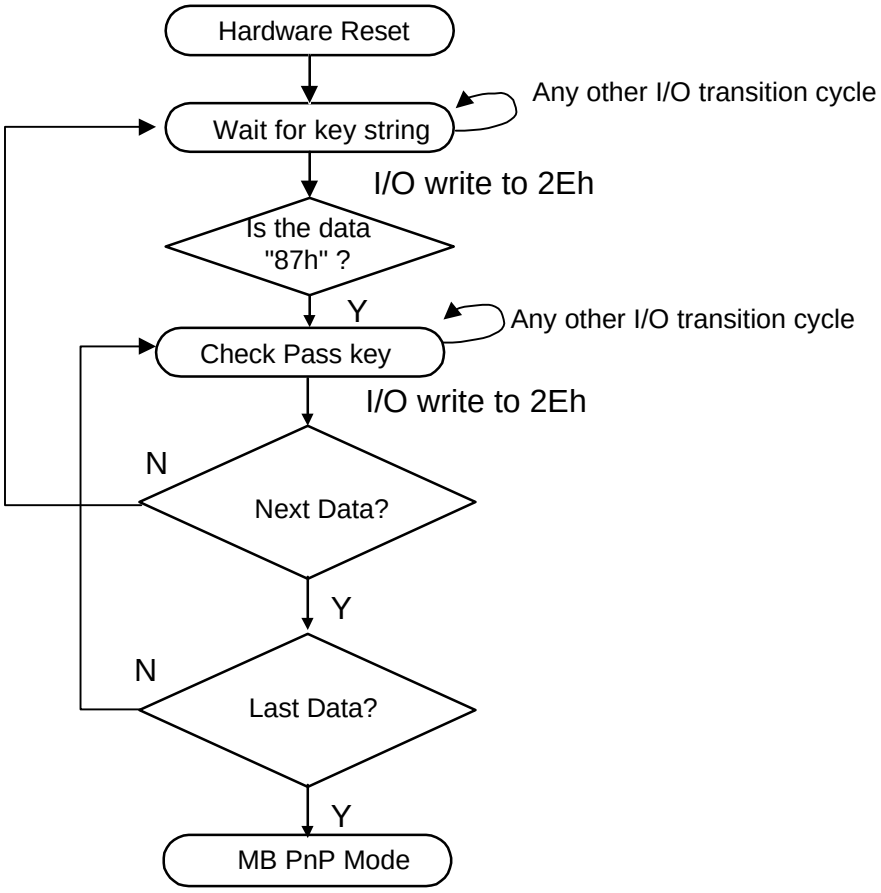
Table 7-1. Power On Strapping Options

	Symbol	Description
JP1	Flash_Seg1	Flash ROM Interface Address Segment 1 (FFFF0000h-FFFFFFFFh, FFFE0000h-FFFEFFFFh) Enable.
JP2	Flash_Seg2	Flash ROM Interface Address Segment 2 (FFEF0000h-FFEFFFFh, FFEE0000h-FFEEFFFFh) Enable.
JP3	Flash_Seg3	Flash ROM Interface Address Segment 3 (FFF80000h-FFFDFFFFh, FFFE0000h-FFFEFFFFh) Enable.
JP4	Flash_Seg4	Flash ROM Interface Address Segment 4 (000F0000h-000FFFFFh, 000E0000h-000EFFFFh) Enable.
JP5	4M_Flash_En	4M Flash ROM Enable (Pin 75 is selected as FA18).
JP6	Chip_sel	Chip selection in Configuration.

8. Configuration

8.1 Configuring Sequence Description

After the hardware reset or power-on reset, the IT8705F enters the normal mode with all logical devices disabled.



There are three steps to completing the Motherboard mode of configuration. Step one is to enter the MB PnP mode. Step two is modifying the data of configuration registers. Step three is exiting the MB PnP mode. These three steps are explained below. Please note that step three must be followed or an undefined state will occur.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, 4 special I/O write operations must be performed during Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four I/O write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) as required in the next step.

	Address Port	Data Port
87h, 01h, 55h, 55h;	2Eh	2Fh
or 87h, 01h, 55h, AAh;	4Eh	4Fh

(2) Modifying the Data of the Configuration Registers

Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global Configuration registers. All registers can be accessed in this mode.

(3) Exit the MB PnP Mode

Set bit 1 of the Configure Control Register (Index: 02h) to "1" to exit the MB PnP mode.

8.2 Description of the Configuration Registers

All the registers will be reset to the default states when RESET is activated, except EC's PME registers.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number(LDN)
All	20h	RO	87h	Chip ID Byte 1
All	21h	RO	05h	Chip ID Byte 2
All	22h	W-RO	00h	Configuration Select and Chip Version
All	23h	R/W	00h	Software Suspend
All	24h	R/W	-	Clock Selection and Flash ROM I/F Control Register
05h[*1]	25h	R/W	00h	GPIO Set 1 Multi-Function Pin Selection Register
05h[*1]	26h	R/W	00h	GPIO Set 2 Multi-Function Pin Selection Register
05h[*1]	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
05h[*1]	28h	R/W	FFh	GPIO Set 4 Multi-Function Pin Selection Register
05h[*1]	29h	R/W	E0h	GPIO Set 5 Multi-Function Pin Selection Register
05h[*1]	2Ah	R/W	FFh	GPIO Set 6 Multi-Function Pin Selection Register
F4h[*1]	2Eh	R/W	00h	Test Mode Register 1
F4h[*1]	2Fh	R/W	00h	Test Mode Register 2

Table 8-2. FDC Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Table 8-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register

Table 8-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	50h	Serial Port 2 Special Configuration Register 2
02h	F2h	R/W	00h	Serial Port 2 Special Configuration Register 3
02h	F3h	R/W	7Fh	Serial Port 2 Special Configuration Register 4

Table 8-5. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	64h	R/W	00h	POST Data Port Base Address MSB Register
03h	65h	R/W	80h	POST Data Port Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select[*2]
03h	F0h	R/W	03h[*3]	Parallel Port Special Configuration Register

Table 8-6. Environment Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
04h	30h	R/W	00h	Environment Controller Activate
04h	60h	R/W	02h	Environment Controller Primary Base Address MSB Register
04h	61h	R/W	90h	Environment Controller Primary Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	Environment Controller Interrupt Level Select
04h	F0h	R/W	00h	PME Event Enable Register
04h	F1h	R/W	00h	PME Status Register
04h	F2h	R/W	00h	PME Control Register 1
04h	F3h	R/W	00h	Environment Controller Special Configuration Register
04h	F4h	R-R/W	00h	PME Control Register 2
04h	F5h	R/W	-	PME Special Code Index Register
04h	F6h	R/W	-	PME Special Code Data Register

Table 8-7. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
05h	60h	R/W	00h	Simple I/O Base Address MSB Register
05h	61h	R/W	00h	Simple I/O Base Address LSB Register
05h	62h	R/W	00h	Panel Button De-bounce Base Address MSB Register
05h	63h	R/W	00h	Panel Button De-bounce Base Address LSB Register
05h	64h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
05h	65h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
05h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
05h	71h	R/W	00h	IRQ Routing Input 0 and 1Interrupt Level Select Register
05h	72h	R/W	00h	IRQ Routing Input 2 and 3 Interrupt Level Select Register
05h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
05h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
05h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
05h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
05h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
05h	B5h	R/W	00h	GPIO Set 6 Pin Polarity Register
05h	B8h	R/W	00h	GPIO Set 1 Pin Internal Pull-up Enable Register
05h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
05h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
05h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
05h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
05h	BDh	R/W	00h	GPIO Set 6 Pin Internal Pull-up Enable Register
05h	C0h	R/W	00h	Simple I/O Set 1 Enable Register
05h	C1h	R/W	00h	Simple I/O Set 2 Enable Register
05h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
05h	C3h	R/W	00h	Simple I/O Set 4 Enable Register

Table 8-7. GPIO Configuration Registers [cont' d]

LDN	Index	R/W	Reset	Configuration Registers or Action
05h	C4h	R/W	00h	Simple I/O Set 5 Enable Register
05h	C5h	R/W	00h	Simple I/O Set 6 Enable Register
05h	C8h	R/W	00h	Simple I/O Set 1 Output Enable Register
05h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
05h	CAh	R/W	00h	Simple I/O Set 3 Output Enable Register
05h	CBh	R/W	00h	Simple I/O Set 4 Output Enable Register
05h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register
05h	CDh	R/W	00h	Simple I/O Set 6 Output Enable Register
05h	D0h	R/W	00h	Panel Button De-bounce Control Register
05h	D1h	R/W	00h	Panel Button De-bounce Set 1 Enable Register
05h	D2h	R/W	00h	Panel Button De-bounce Set 2 Enable Register
05h	D3h	R/W	00h	Panel Button De-bounce Set 3 Enable Register
05h	D4h	R/W	00h	Panel Button De-bounce Set 4 Enable Register
05h	D5h	R/W	00h	Panel Button De-bounce Set 5 Enable Register
05h	D6h	R/W	00h	Panel Button De-bounce Set 6 Enable Register
05h	F0h	R/W	00h	SMI# Control Register
05h	F1h	R/W	00h	Reserved
05h	F2h	R/W	00h	SMI# Status Register
05h	F5h	R/W	00h	SMI# Pin Mapping
05h	F6h	R/W	00h	Hardware Monitor Alert Beep Pin Mapping Register
05h	F7h	R/W	00h	GP LED Blinking 1 Pin Mapping Register
05h	F8h	R/W	00h	GP LED Blinking 1 Control Register
05h	F9h	R/W	00h	GP LED Blinking 2 Pin Mapping Register
05h	FAh	R/W	00h	GP LED Blinking 2 Control Register
05h	FBh	R/W	00h	Watch Dog Timer Control Register
05h	FCh	R/W	00h	Watch Dog Timer Time-out output Pin Mapping Register
05h	FDh	R/W	00h	Watch Dog Timer Time-out Value Register
05h	FEh	RO	--	VID Input Register
05h	FFh	R/W	00h	VID Output Register

Table 8-8. Game Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
06h	30h	R/W	00h	Game Port Activate
06h	60h	R/W	02h	Game Port Base Address MSB Register
06h	61h	R/W	01h	Game Port Base Address LSB Register

Table 8-9. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
07h	30h	R/W	00h	Consumer IR Activate
07h	60h	R/W	03h	Consumer IR Base Address MSB Register
07h	61h	R/W	10h	Consumer IR Base Address LSB Register
07h	70h	R/W	0Bh	Consumer IR Interrupt Level Select
07h	F0h	R/W	00h	Consumer IR Special Configuration Register

Table 8-10. MIDI Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
08h	30h	R/W	00h	MIDI Port Activate
08h	60h	R/W	03h	MIDI Port Base Address MSB Register
08h	61h	R/W	00h	MIDI Port Base Address LSB Register
08h	70h	R/W	0Ah	MIDI Port Interrupt Level Select
08h	F0h	R/W	00h	MIDI Port Special Configuration Register

Notes:

*1: All these registers can be read from all LDNs.

*2: When the ECP mode is not enabled, this register is **read only** as "04h", and cannot be written.

*3: When the bit 2 of the base address of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

8.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 8-11. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0 FDC	Base + (2 - 5) and + 7	
LDN=1 SERIAL PORT 1	Base + (0 -7)	
LDN=2 SERIAL PORT 2	Base1 + (0 -7)	COM Port
LDN=3 PARALLEL PORT	Base1 + (0 -3) Base1 + (0 -7) Base1 + (0 -3) and Base2 + (0 -3) Base1 + (0 -7) and Base2 + (0 -3) Base3	SPP SPP+EPP SPP+ECP SPP+EPP+ECP POST Data Port
LDN=4 Environment Controller	Base1 + (0 -7) Base2 + (0 -3)	Environment Controller PME#
LDN=5 GPIO		-
LDN=6 Game Port	Base + (0 -1)	-
LDN=7 Consumer IR	Base + (0 -7)	-
LDN=8 MIDI Port	Base + (0 -1)	-

8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	**Reserved**
1	**Return to the "Wait for Key" state.** This bit is used when the configuration sequence is completed.
0	Reset all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This **read/write** register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, the ACTIVATE command is only effective for the selected logical devices.

8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)

This **read only** register is the Chip ID Byte 1. Bits [7:0]=87h when read.

8.3.4 Chip ID Byte 2 (Index=21h, Default=05h)

This **read only** register is the Chip ID Byte 2. Bits [7:0]=05h when read.

8.3.5 Configuration Select and Chip Version (Index=22h, Default=02h)

Bit	Description
7	**Configuration Select** This bit is used to select the chip, which needed to be configured. When there are two IT8705F chips in a system, to write "1" this bit will select JP6=1 (power-on strapping value of RTS2#) to be configured. The chip with JP6=0 will exit the configuration mode. To write "0", the chip with JP6=0 will be configured and the chip with JP6=0 will exit. If no write on this register, both chips will be configured.
6-4	**Reserved**
3-0	**Version**

8.3.6 Software Suspend (Index=23h, Default=00h)

Bit	Description
7-6	**SCRPRES# Select** 00: Pin 81 01: Pin 79 10: Pin 75 11: Pin 74
5-4	**Reserved**
0	**Software Suspend** This register is the Software Suspend register. When the bit 0 is set, the IT8705F enters the "Software Suspend" state. All the devices remain inactive until this bit is cleared or when the wake-up event occurs. The wake-up event occurs at any transition on signals RI1# (pin 119) and RI2# (pin 127).

8.3.7 Clock Selection and Flash ROM I/F Control Register (Index=24h, Default=ssssss000b)

The default values of bits 7-3 depend on the power-on strapping of JP1-5.

Bit	Description
7	**Flash ROM Interface Address Segment 4 (000F0000h-000FFFFFh, 000E0000h-000EFFFFh) Enable**
6	**Flash ROM Interface Address Segment 3 (FFF80000h-FFFDFFFFh, FFFE0000h-FFFEFFFFh) Enable**
5	**Flash ROM Interface Address Segment 2 (FFEF0000h-FFEFFFFh, FFEE0000h-FFEEFFFFh) Enable**
4	**Flash ROM Interface Address Segment 1 (FFFF0000h-FFFFFFFFh, FFFE0000h-FFFEFFFFh) Enable**
3	**4M bits Flash ROM Enable (Pin 75 is selected as FA18)**
2	**Flash ROM I/F Writes Enable**
1	**Reserved**
0	**CLKIN Frequency** 0: 48 MHz. 1: 24 MHz.

8.3.8 GPIO Set 1 Multi-Function Pin Selection Register (Index=25h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 14** 0: Select the Flash ROM Interface Data 7. 1: Select the General Purpose I/O 17.
6	**Perform the function selection of pin 13** 0: Select the Flash ROM Interface Data 6. 1: Select the General Purpose I/O 16.
5	**Perform the function selection of pin 12** 0: Select the Flash ROM Interface Data 5. 1: Select the General Purpose I/O 15.
4	**Perform the function selection of pin 11** 0: Select the Flash ROM Interface Data 4. 1: Select the General Purpose I/O 14.
3	**Perform the function selection of pin 10** 0: Select the Flash ROM Interface Data 3. 1: Select the General Purpose I/O 13.
2	**Perform the function selection of pin 9** 0: Select the Flash ROM Interface Data 2. 1: Select the General Purpose I/O 12.
1	**Perform the function selection of pin 8** 0: Select the Flash ROM Interface Data 1. 1: Select the General Purpose I/O 11.
0	**Perform the function selection of pin 7** 0: Select the Flash ROM Interface Data 0. 1: Select the General Purpose I/O 10.

8.3.9 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 23** 0: Select the Flash ROM Interface Address 7. 1: Select the General Purpose I/O 27.
6	**Perform the function selection of pin 22** 0: Select the Flash ROM Interface Address 6. 1: Select the General Purpose I/O 26.
5	**Perform the function selection of pin 21** 0: Select the Flash ROM Interface Address 5. 1: Select the General Purpose I/O 25.
4	**Perform the function selection of pin 20** 0: Select the Flash ROM Interface Address 4. 1: Select the General Purpose I/O 24.
3	**Perform the function selection of pin 19** 0: Select the Flash ROM Interface Address 3. 1: Select the General Purpose I/O 23.
2	**Perform the function selection of pin 18** 0: Select the Flash ROM Interface Address 2. 1: Select the General Purpose I/O 22.
1	**Perform the function selection of pin 17** 0: Select the Flash ROM Interface Address 1. 1: Select the General Purpose I/O 21.
0	**Perform the function selection of pin 16** 0: Select the Flash ROM Interface Address 0. 1: Select the General Purpose I/O 20.

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 31** 0: Select the Flash ROM Interface Address15. 1: Select the General Purpose I/O 37.
6	**Perform the function selection of pin 30** 0: Select the Flash ROM Interface Address 14. 1: Select the General Purpose I/O 36.
5	**Perform the function selection of pin 29** 0: Select the Flash ROM Interface Address13. 1: Select the General Purpose I/O 35.

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h) [cont' d]

Bit	Description
4	**Perform the function selection of pin 28** 0: Select the Flash ROM Interface Address 12. 1: Select the General Purpose I/O 34.
3	**Perform the function selection of pin 27** 0: Select the Flash ROM Interface Address 11. 1: Select the General Purpose I/O 33.
2	**Perform the function selection of pin 26** 0: Select the Flash ROM Interface Address 10. 1: Select the General Purpose I/O 32.
1	**Perform the function selection of pin 25** 0: Select the Flash ROM Interface Address 9. 1: Select the General Purpose I/O 31.
0	**Perform the function selection of pin 24** 0: Select the Flash ROM Interface Address 8. 1: Select the General Purpose I/O 30.

8.3.11 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=FFh)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 56** 0: Select the Joystick B Button 2. 1: Select the General Purpose I/O 47.
6	**Perform the function selection of pin 55** 0: Select the Joystick B Button 1. 1: Select the General Purpose I/O 46.
5	**Perform the function selection of pin 54** 0: Select the Joystick B Coordinate Y. 1: Select the General Purpose I/O 45.
4	**Perform the function selection of pin 53** 0: Select the Joystick B Coordinate X. 1: Select the General Purpose I/O 44.
3	**Perform the GP43 function of pin 52** 0: Select the Joystick A Button 2. 1: Select the General Purpose I/O 43.
2	**Perform the function selection of pin 51** 0: Select the Joystick A Button 1. 1: Select the General Purpose I/O 42.
1	**Perform the function selection of pin 50** 0: Select the Joystick A Coordinate Y. 1: Select the General Purpose I/O 41.
0	**Perform the function selection of pin 49** 0: Select the Joystick A Coordinate X. 1: Select the General Purpose I/O 40.

8.3.12 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=E0h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 75** If 4M bits Flash ROM (bit 3 of Index 24h register) is enabled, this bit is no used. 0: Select the Fan Tachometer Input 3. 1: Select the General Purpose I/O 57.
6	**Perform the function selection of pin 74** 0: Select the Fan Tachometer Input 2. 1: Select the General Purpose I/O 56.
5	**Perform the function selection of pin 73** 0: Select the Fan Tachometer Input 1. 1: Select the General Purpose I/O 55.
4	**Perform the function selection of pin 48** 0: Select the Flash ROM Interface Write Enable #. 1: Select the General Purpose I/O 54.
3	**Perform the function selection of pin 47** 0: Select the Flash ROM Interface Chip Select #. 1: Select the General Purpose I/O 53.
2	**Perform the function selection of pin 34** 0: Select the Flash ROM Interface Read Strobe #. 1: Select the General Purpose I/O 52.
1	**Perform the function selection of pin 33** 0: Select the Flash ROM Interface Address 17. 1: Select the General Purpose I/O 51.
0	**Perform the function selection of pin 32** 0: Select the Flash ROM Interface Address 16. 1: Select the General Purpose I/O 50.

8.3.13 GPIO Set 6 Multi-Function Pin Selection Register (Index=2Ah, Default=FFh)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 85** 0: Select the Consumer Infrared Receive Input (if bit 6 of PCR2 is low) or MIDI Input (if bit 6 of PCR2 is high). 1: Select the General Purpose I/O 67.
6	**Perform the function selection of pin 84** 0: Select the Consumer Infrared Transmit Output (if bit 6 of PCR2 is low) or MIDI Output (if bit 6 of PCR2 is high). 1: Select the General Purpose I/O 66.
5	**Perform the function selection of pin 83** 0: Select the Infrared Receive Input. 1: Select the General Purpose I/O 65.
4	**Perform the function selection of pin 82** 0: Select the Infrared Transmit Output. 1: Select the General Purpose I/O 64.
3	**Perform the function selection of pin 81** 0: Select the Power Management Event #. 1: Select the General Purpose I/O 63.
2	**Perform the function selection of pin 80** 0: Select the Fan Control Output 3. 1: Select the General Purpose I/O 62.
1	**Perform the function selection of pin 79** 0: Select the Fan Control Output 2. 1: Select the General Purpose I/O 61.
0	**Perform the function selection of pin 78** 0: Select the Fan Control Output 1. 1: Select the General Purpose I/O 60.

8.3.14 Test Mode Register 1 (Index=2Eh, Default=00h)

This register is the Test 1 Register and is reserved for ITE. It should not be set.

8.3.15 Test Mode Register 2 (Index=2Fh, Default=00h)

This register is the Test 2 Register and is reserved for ITE. It should not be set.

8.4 FDC Configuration Registers (LDN=00h)

8.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**FDC Enable** 0: Disabled. 1: Enabled.

8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only, with "0h" for Base Address [15:12]**
3-0	**FDC Base Address MSB** Mapped as Base Address [11:8].

8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	**FDC Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**FDC Interrupt Level Select** Select the interrupt level note1 for FDC.

8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	**Reserved** with default "00h".
2-0	**FDC DMA Channel Select** Select the DMA channel note2 for FDC.

8.4.6 FDC Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-4	**Reserved** with default "00h".
3	**FDC IRQ Sharing** 1: IRQ sharing. 0: Normal IRQ.
2	**Floppy A/B Swap** 1: Swap Floppy Drives A, B. 0: Normal.
1	**3 mode/AT Mode** 1: 3-mode. 0: AT mode.
0	**Software Write Protect** 1: Software Write Protect. 0: Normal.

8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)

Bit	Description
7-4	**Reserved** with default "0000b".
3-2	**FDD B Data Rate Table Select (DRT1-0)**
1-0	**FDD A Data Rate Table Select (DRT1-0)**

8.5 Serial Port 1 Configuration Registers (LDN=01h)

8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 1 Enable** 1: Enabled. 0: Disabled.

8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Serial Port 1 Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Serial Port 1 Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only as "000b".**

8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	**Reserved:** default = "0h."
3-0	**Serial Port 1 Interrupt Level Select** Select the interrupt level [note1] for Serial Port 1.

8.5.5 Serial Port 1 Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-3	**Reserved:** default = "00h".
2-1	**Clock Source** 00: 24 MHz/13 (Standard). Others: Reserved.
0	**IRQ Sharing Enable** 1: IRQ sharing. 0: Normal.

8.6 Serial Port 2 Configuration Registers (LDN=02h)

8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 2 Enable** 1: Enabled. 0: Disabled.

8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only:** with "0h" for Base Address[15:12].
3-0	**Serial Port 2 Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Serial Port 2 Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only:** as "000b".

8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**Serial Port 2 Interrupt Level Select** Select the interrupt level [note1] for Serial Port 2.

8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-3	**Reserved:** with default "00h".
2-1	**Clock Source** 00: 24 MHz/13 (Standard). Others: Reserved.
0	**IRQ Sharing Enable** 1: IRQ sharing. 0: Normal.

8.6.6 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	**IR Rx2Tx Delay Mode** 1:No transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode. 0: Transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode.
6	**IR Tx2Rx Delay Mode** 1: No reception delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode. 0: Reception delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode.
5	**Reserved**
4	**Half Duplex Enable** 1: Half Duplex (default). 0: Full Duplex.
3	**Reserved**
2-0	**UART 2 Function Select** 000: Standard 001: IrDA SIR 010: ASKIR 100 : Smart Card Reader (SCR) Others: Reserved

8.6.7 Serial Port 2 Special Configuration Register 3 (Index=F2h, Default=00h)

Bit	Description
7	**COM_PNP_EN** 0: Disable COM Port device Plug-and-Play operation (default). 1: Enable COM Port device Plug-and-Play operation.
6-5	**Reserved**
4	**PNP_ID** This bit is only available when bit 7=1. 0: PNP_ID Access mode (default). 1: Normal Plug-and-Play operation mode.
3	**Reserved**
2	**SCPFET# Polarity** 0: Active low (default). 1: Active high.
1-0	**SCR Clock Select** 00: Stop 01: 3.5 MHz 10: 7.1 MHz 11: Special Divisor (96 MHz/DIV96M)

8.6.8 Serial Port 2 Special Configuration Register 4 (Index=F3h, Default=7Fh)

Bit	Description
7	**Reserved**
6-0	**SCR Clock Special Divisor (DIV96M)** When the SCR Clock Select is 11b, the SCCLK output clock frequency is 96MHz / DIV96M.

8.7 Parallel Port Configuration Registers (LDN=03h)

8.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Parallel Port Enable** 1: Enabled. 0: Disabled.

8.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If the bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	**Base Address LSB** **Read/write**, mapped as Base Address[7:2].
1-0	**Read only** as "00b".

8.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Secondary Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	**Secondary Base Address LSB** **Read/write**, mapped as Base Address[7:2].
1-0	**Read only** as "00b".

8.7.6 POST Data Port Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**POST Data Port Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.7.7 POST Data Port Base Address LSB Register (Index=65h, Default=80h)

Bit	Description
7-0	**POST Data Port Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.7.8 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**Interrupt Level Select** Select the interrupt level [note1] for Parallel Port.

8.7.9 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	**Reserved** with default "00h".
2-0	**DMA Channel Select** Select the DMA channel note2 for Parallel Port.

8.7.10 Parallel Port Special Configuration Register (Index=F0h, Default=03h)

Bit	Description
7-4	**Reserved**
3	**POST Data Port Disable** 1: POST Data Port Disable. 0: POST Data Port Enable.
2	**IRQ Sharing Enable** 1: IRQ sharing. 0: Normal.
1-0	**Parallel Port Mode** 00: SPP (Standard Parallel Port mode) 01: SPP & EPP (Enhanced Parallel Port) 10: SPP & ECP (Extended Capabilities Parallel Port) 11: SPP & EPP & ECP

If the bit 1 is set, ECP mode is enabled. If the bit 0 is set, EPP mode is enabled. These two bits are independent. However, according to the EPP spec., when Parallel Port Primary Base Address bit 2 is set to 1, the EPP mode cannot be enabled.

8.8 Environment Controller Configuration Registers (LDN=04h)

8.8.1 Environment Controller Activate Register (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Environment Controller Enable** 1: Enabled. 0: Disabled.

8.8.2 Environment Controller Primary Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**E.C. Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.8.3 Environment Controller Primary Base Address LSB Register (Index=61h, Default=90h)

Bit	Description
7-3	**E.C. Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

8.8.4 PME Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**PME Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.8.5 PME Direct Access Base Address LSB Register (Index=63h, Default=30h)

Bit	Description
7-3	**PME Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

8.8.6 Environment Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**E.C. Interrupt Level Select** Select the interrupt level [note1] for Environment Controller.

8.8.7 PME Event Enable Register (Index=F0h, Default=00h)

Bit	Description
7	It is set to 1 when VCCH is OFF. Writing 1 to clear this bit. This bit is ineffective when a "0" is written to this bit.
6-3	**Reserved**
2	**RI2# Event Enable** 1: RI2# event enabled. 0: RI2# event disabled.
1	**RI1# Event Enable** 1: RI1# event enabled. 0: RI1# event disabled.
0	**CIR Event Enable** 1: CIR event enabled. 0: CIR event disabled.

8.8.8 PME Status Register (Index=F1h, Default=00h)

Bit	Description
7	It is set to 1 when VCC is ON during previous AC power failure, and 0 when VCC power is OFF.
6-3	**Reserved**
2	**RI2# Event Detected** 1: RI2# event detected. 0: RI2# event undetected.
1	**RI1# Event Detected** 1: RI1# event detected. 0: RI1# event undetected.
0	**CIR Event Detected** 1: CIR event detected. 0: CIR event undetected.

8.8.9 PME Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	**PER and PSR Normal Run Access Enable**
6-0	**Reserved**

8.8.10 Environment Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**EC IRQ Sharing Enable** 1: IRQ sharing. 0: Normal.

8.8.11 PME Control Register 2 (PCR2) (Index=F4h, Default=00h)

Bit	Description
7	**Reserved**
6	**This bit is active when the related pins are not selected as GPIO function.** 1: SIR/ASKIR and CIR ports use the same pins (Pin 82 and Pin 83). Pins 84 and 85 are defined at MIDI port. 0: Pins 82 and 83 are defined at SIR/ASKIR port, and pins 84 and 85 are defined at CIR port.
5-0	**Reserved**

8.8.12 PME Special Code Index Register (Index=F5h)

Bit	Description
7-6	**Reserved** (should be filled "00b").
5-0	Indicate which Identification Key Code or CIR code register is to be read/written via 0xF6.

8.8.13 PME Special Code Data Register (Index=F6h)

There are 20 CIR event codes (Index 20h-32h) stored in this port. The index pointer is changed by PME Special Code Index Register. The first byte (Index 20h) is used to specify the pattern length in bytes. Bits[7:4] are used when VCC is ON, and bits[3:0] are used when VCC goes OFF. The minimum byte number is 3 (when bits[7:4] or bits[3:0]=0h), and the maximum byte number is 18 (when bits[7:4] or bits[3:0] =Fh).

8.9 GPIO Configuration Registers (LDN=05h)

8.9.1 Simple I/O Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**Simple IO Base Address MSB** **Read/write**, mapped as Base Address [11:8].

8.9.2 Simple I/O Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-0	**Simple IO Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.9.3 Panel Button De-bounce Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**P.B.D Base Address MSB** **Read/write**, mapped as Base Address [11:8].

8.9.4 Panel Button De-bounce Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	**P.B.D Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.9.5 SMI# Normal Run Access Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**SMI Base Address MSB** **Read/write**, mapped as Base Address [11:8].

8.9.6 SMI# Normal Run Access Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-0	**SMI Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.9.7 Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)

Bit	Description
7-4	**Reserved**
3-0	**P.B.D Interrupt Level Select** Select the interrupt level note1 for Panel Button De-bounce.

8.9.8 IRQ Routing Input 0 and 1 Interrupt Level Select Register (Index=71h, Default=00h)

Bit	Description
7-4	**IRQIN1 Interrupt Level Select** Select the interrupt level note1 for IRQIN1.
3-0	**IRQIN0 Interrupt Level Select** Select the interrupt level note1 for IRQIN0.

8.9.9 IRQ Routing Input 2 and 3 Interrupt Level Select Register (Index=72h, Default=00h)

Bit	Description
7-4	**IRQIN3 Interrupt Level Select** Select the interrupt level note1 for IRQIN3.
3-0	**IRQIN2 Interrupt Level Select** Select the interrupt level note1 for IRQIN2.

8.9.10 GPIO Pin Set 1, 2, 3, 4, 5 and 6 Polarity Registers (Index=B0h, B1h, B2h, B3h, B4h and B5h, Default=00h)

These registers are used to program the GPIO pin type as either polarity inverting or non-inverting.

Bit	Description
7-0	**GPIO Polarity Inverting** For each bit: 1: GPIO pin type is polarity inverting. 0: GPIO pin type is polarity non-inverting.

8.9.11 GPIO Pin Set 1, 2, 3, 4, 5 and 6 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh, BCh and BDh, Default=00h)

These registers are used to enable the GPIO pin internal pull-up.

Bit	Description
7-0	**GPIO Pull-up Enable** For each bit: 1: Enable GPIO pin internal pull-up. 0: Disable GPIO pin internal pull-up.

8.9.12 Simple I/O Set 1, 2, 3, 4, 5 and 6 Enable Registers (Index=C0h, C1h, C2h, C3h,C4h and C5h, Default=00h)

These registers are used to select the functions of either the Simple I/O or the Alternate function.

Bit	Description
7-0	**Simple GPIO Enable** For each bit: 1: Select the Simple I/O function. 0: Select the Alternate function.

8.9.13 Simple I/O Set 1, 2, 3, 4, 5 and 6 Output Enable Registers (Index=C8h,C9h,CAh,CBh,CCh and CDh, Default=00h)

These registers are used to determine the direction of the Simple I/O.

Bit	Description
7-0	**GPIO Output Enable** For each bit: 0: The direction of the Simple I/O is input mode. 1: The direction of the Simple I/O is output mode.

8.9.14 Panel Button De-bounce Control Register (Index=D0h, Default=00h)

Bit	Description
7-5	**Reserved**
4	**IRQ Sharing** 0: Disabled. 1: Enabled.
3	**IRQ Output Type** 0: Edge. 1: Level.
2	**IRQ Output Enable** 0: Disabled. 1: Enabled.
1-0	**De-bounce Time Selection** 00: 8 ms (6 ms ignored, 8 ms passed) 01: 16 ms (12 ms ignored, 16 ms passed) 10: 32 ms (24 ms ignored, 21 ms passed) 11: 64 ms (48 ms ignored, 64 ms passed)

8.9.15 Panel Button De-bounce Set 1, 2, 3, 4, 5 and 6 Enable Registers (Index=D1h, D2h, D3h, D4h, D5h and D6h, Default=00h)

These registers are used to enable Panel Button De-bounce for each pin.

Bit	Description
7-0	**P.B.D Enable** For each bit: 1: Enable Panel Button De-bounce. 0: Disable Panel Button De-bounce

8.9.16 SMI# Control Register (Index=F0h, Default=00h)

Bit	Description
7	**Reserved**
6	**SMI# of MIDI IRQ Enable** Enable the generation of an SMI# due to MIDI Port's IRQ (EN_CIRQ).
5	**SMI# of CIR IRQ Enable** Enable the generation of an SMI# due to CIR's IRQ (EN_CIRQ).
4	**SMI# of EC IRQ Enable** Enable the generation of an SMI# due to Environment Controller's IRQ (EN_ECIRQ).
3	**SMI# of PPORT IRQ Enable** Enable the generation of an SMI# due to Parallel Port's IRQ (EN_PIRQ).
2	**SMI# of UART2 IRQ Enable** Enable the generation of an SMI# due to Serial Port 2's IRQ (EN_S2IRQ).
1	**SMI# of UART1 IRQ Enable** Enable the generation of an SMI# due to Serial Port 1's IRQ (EN_S1IRQ).
0	**SMI# of FDC IRQ Enable** Enable the generation of an SMI# due to FDC's IRQ (EN_FIRQ).

8.9.17 SMI# Status Register (Index=F2h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7	**Reserved**
6	The generation of an SMI# due to MIDI Port's IRQ.
5	The generation of an SMI# due to CIR's IRQ.
4	The generation of an SMI# due to Environment Controller's IRQ.
3	The generation of an SMI# due to Parallel Port's IRQ.
2	The generation of an SMI# due to Serial Port 2's IRQ.
1	The generation of an SMI# due to Serial Port 1's IRQ.
0	The generation of an SMI# due to FDC's IRQ.

8.9.18 SMI# Pin Mapping Register (Index=F5h, Default=00h)

Bit	Description
7	**Reserved**
6	**SMI# Direct Access Enable** 0: Disable SMI# Direct Access (default) 1: Enable SMI# Direct Access.
5-0	**SMI# Pin Location** Please see Location mapping table note3.

8.9.19 Hardware Monitor Alert Beep Pin Mapping Register (Index=F6h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Hardware Monitor Alert Beep Pin Location** Please see Location mapping table note3.

8.9.20 GP LED Blinking 1 Pin Mapping Register (Index=F7h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 1 Pin Location** Please see Location mapping table note3.

8.9.21 GP LED Blinking 1 Control Register (Index=F8h, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 1 Active Pulse Control** 0: 1/2 duty (default) 1: short active pulse.
2-1	**GP LED Blinking 1 Frequency Select** 00: 4 Hz (default) 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 1 Active Mode** 0: Blinking mode (default). 1: Always active.

8.9.22 GP LED Blinking 2 Pin Mapping Register (Index=F9h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 2 Pin Location** Please see Location mapping table note3.

8.9.23 GP LED Blinking 2 Control Register (Index=FAh, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 2 Active Pulse Control** 0: 1/2 duty (default). 1: short active pulse.
2-1	**GP LED Blinking 2 Frequency Select** 00: 4 Hz (default) 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 2 Active Mode** 0: Blinking mode (default). 1: Always active.

8.9.24 Watch Dog Timer Control Register (Index=FBh, Default=00h)

Bit	Description
7	**CIR Interrupt to Reset WDT Counter Enable** 0: Disable a CIR Interrupt to reset WDT Counter (default). 1: Enable a CIR Interrupt to reset WDT Counter.
6-5	**Reserved**
4	**A read from or write to the Game Port Base Address to Reset WDT Counter Enable** 0: Disable a read from or write to Game port base address to reset WDT Counter (default). 1: Enable a read from or write to Game port base address to reset WDT Counter.
3	**WDT Counter Unit Select** 0: Minute (default). 1: Second.
2	**Reserved**
1	**Direct Time Out Control** This bit is self-clearing. 0: Normal (default). 1: Direct Time out regardless of the counter.
0	**WDT Status** 0: No time-out after last re-load counter value (default). 1: The timer was time-out.

8.9.25 Watch Dog Timer Time-out Output Pin Mapping Register (Index=FCh, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Watch Dog Timer Time-out Output Pin Location** Please see Location mapping table note3.

8.9.26 Watch Dog Timer Time-out Value Register (Index=FDh, Default=00h)

Bit	Description
7-0	**Watch Dog Timer Time-out Value** Watch Dog Timer Counter Time-out value (1~256 unit(s)).

8.9.27 VID Input Register (Index=FEh, Default= --)

Bit	Description
7-5	**Reserved**
4-0	**VID_I[4:0]** These bits are read-only. When read, they will perform the states of pins VID_I[4:0].

8.9.28 VID Output Register (Index=FFh, Default=00h)

Bit	Description
7	**VID_O[4:0] Output Select** 0: Translate VID_I[4:1] directly (default). 1: Output the desired value (bits [4:0] of this register).
6-5	**Reserved**
4-0	**Output Value of VID_O[4:0]** These bits are desired output value of VID_O[4:0].

8.10 Game Port Configuration Registers (LDN=06h)

8.10.1 Game Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Game Port Enable** 1: Enabled. 0: Disabled.

8.10.2 Game Port Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**Game Port Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.10.3 Game Port Base Address LSB Register (Index=61h, Default=01h)

Bit	Description
7-0	**Game Port Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.11 Consumer IR Configuration Registers (LDN=07h)

8.11.1 Consumer IR Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Consumer IR Enable** 1: Enabled. 0: Disabled.

8.11.2 Consumer IR Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**CIR Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.11.3 Consumer IR Base Address LSB Register (Index=61h, Default=10h)

Bit	Description
7-3	**CIR Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

8.11.4 Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**CIR Interrupt Level Select** Select the interrupt level note1 for Consumer IR.

8.11.5 Consumer IR Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-1	**Reserved** with default "00h".
0	1: IRQ sharing. 0: Normal.

8.12 MIDI Port Configuration Registers (LDN=08h)

8.12.1 MIDI Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**MIDI Port Enable** 1: Enabled. 0: Disabled.

8.12.2 MIDI Port Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**MIDI Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.12.3 MIDI Port Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-1	**MIDI Base Address LSB** **Read/write**, mapped as Base Address[7:3].
0	**Read only** as "000b".

8.12.4 MIDI Port Interrupt Level Select (Index=70h, Default=0Ah)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**MIDI Port Interrupt Level Select** Select the interrupt level note1 for MIDI port.

8.12.5 MIDI Port Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-6	**MID_IN Location Select** 00: Pin 85. Please refer to Section 6 (default) 01: Pin 79 10: Pin 74 11: Pin 7
5-4	**MID_OUT Location Select** 00: Pin 84. Please refer to Section 6 (default) 01: Pin 78 10: Pin 73 11: Pin 8
3	**FIFO Disable** 0: Enabled (default). 1: Disabled.
2-1	**Receive FIFO Trigger Level** 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
0	**MIDI Port Interrupt Mode Select** 0: Normal (default). 1: IRQ sharing.

Note 1: **Interrupt Level Mapping**

Fh-Dh: not valid
Ch: IRQ12
.
.
3h: IRQ3
2h: not valid
1h: IRQ1
0h: no interrupt selected

Note 2: **DMA Channel Mapping**

7h-5h: not valid
4h: no DMA channel selected
3h: DMA3
2h: DMA2
1h: DMA1
0h: DMA0

Note 3: **Location Mapping Table**

Location	Description
001 000	GP10 (pin 7)
001 001	GP11 (pin 8)
001 010	GP12 (pin 9)
001 011	GP13 (pin 10)
001 100	GP14 (pin 11)
001 101	GP15 (pin 12)
001 110	GP16 (pin 13)
001 111	GP17 (pin 14)
010 000	GP20 (pin 16)
010 001	GP21 (pin 17)
010 010	GP22 (pin 18)
010 011	GP23 (pin 19)
010 100	GP24 (pin 20)
010 101	GP25 (pin 21)
010 110	GP26 (pin 22)
010 111	GP27 (pin 23)
011 000	GP30 (pin 24)
011 001	GP31 (pin 25)
011 010	GP32 (pin 26)
011 011	GP33 (pin 27)
011 100	GP34 (pin 28)
011 101	GP35 (pin 29)

Note 3: **Location Mapping Table [cont'd]**

Location	Description
011 110	GP36 (pin 30)
011 111	GP37 (pin 31)
100 000	GP40 (pin 49)
100 001	GP41 (pin 50)
100 010	GP42 (pin 51)
100 011	GP43 (pin 52)
100 100	GP44 (pin 53)
100 101	GP45 (pin 54)
100 110	GP46 (pin 55)
100 111	GP47 (pin 56)
101 000	GP50 (pin 32)
101 001	GP51 (pin 33)
101 010	GP52 (pin 34)
101 011	GP53 (pin 47)
101 100	GP54 (pin 48)
101 101	GP55 (pin 73)
101 110	GP56 (pin 74)
101 111	GP57 (pin 75)
110 000	GP60 (pin 78), powered by VCCH
110 001	GP61 (pin 79), powered by VCCH
110 010	GP62 (pin 80), powered by VCCH
110 011	GP63 (pin 81), powered by VCCH
110 100	GP64 (pin 82), powered by VCCH
110 101	GP65 (pin 83), powered by VCCH
110 110	GP66 (pin 84), powered by VCCH
110 111	GP67 (pin 85), powered by VCCH
else	Reserved

9. Functional Description

9.1 LPC Interface

The IT8705F supports the peripheral site of the LPC I/F as described in the LPC Interface Specification Rev.1.0 (Sept. 29,1997). In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK (PCICLK)), the IT8705F also supports LDRQ#, SERIRQ and PME#.

9.1.1 LPC Transactions

The IT8705F supports some parts of the cycle types described in the LPC I/F specification. Memory read and Memory write cycles are used for the Flash I/F. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Super I/O module processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will make reactions according to the DMA requests from the DMA devices in the Super I/O modules, and decides whether to ignore the current transaction or not.

The FDC and ECP are 8-bit DMA devices, so if the LPC host initializes a DMA transaction with data size of 16/32 bits, the LPC interface will process the first 8-bit data and response with a SYNC ready (0000b) which will terminate the DMA burst. The LPC interface will then re-issue another LDRQ# message to assert DREQn after finishing the current DMA transaction.

9.1.2 LDRQ# Encoding

The Super I/O module provides two DMA devices: the FDC and the ECP. The LPC Interface provides LDRQ# encoding to reflect the DREQ[3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to track DMA requests rapidly. But, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there is at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages, and sends those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

9.2 Serialized IRQ

The IT8705F conforms to the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature, and is able to interface with most PC chipsets. The IT8705F encodes the parallel interrupts to an SERIRQ which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

9.2.1 Continuous Mode

When in the continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the Turn-around State of current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events, even though no IRQn status is changed. The SERIRQ enter the continuous mode following a system reset.

9.2.2 Quiet Mode

In the Quiet mode, when one SIRQ Slave detects its input IRQn/events have been changed, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence. In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity means low mode power consumption.

9.2.3 Waveform Samples of SERIRQ Sequence

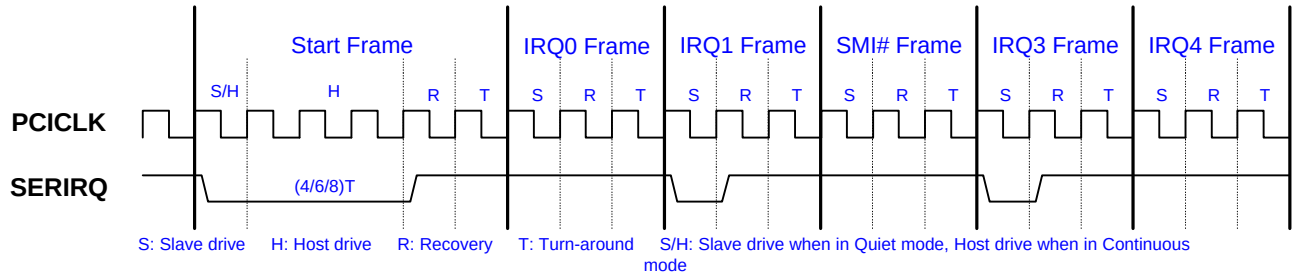


Figure 9-1. Start Frame Timings

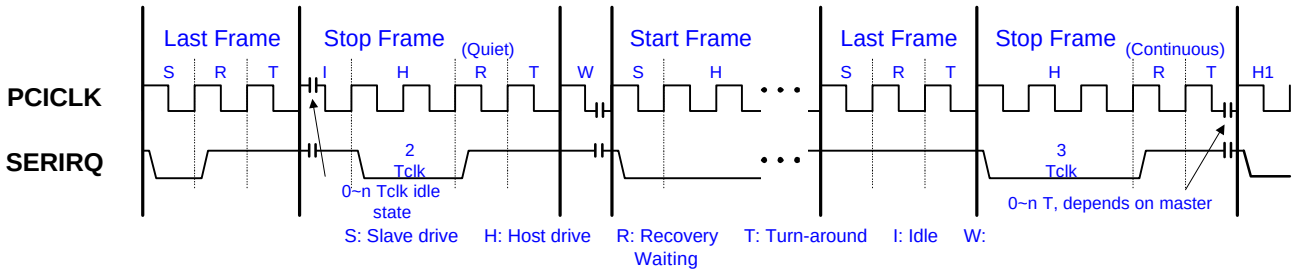


Figure 9-2. Stop Frame Timings

9.2.4 SERIRQ Sampling Slot

Slot Number	IRQn / Events	# of Clocks Past Start	IT8705F
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32-22	Unassigned	95 / 65	-

9.3 General Purpose I/O

The IT8705F provides six sets of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection registers (Index=25h, 26h, 27h, 28h, 29h and 2Ah of the Global Configuration Registers) are set. GPIO function includes the simple I/O function and alternate function, and the function selection is determined by the Simple I/O Enable Registers (LDN=05h, Index=C0h, C1h, C2h, C3h and C4h).

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. The accessed I/O ports are programmable. Base Address is programmed on the GPIO Simple I/O Base Address LSB & MSB registers (LDN=05h, Index=60h and 61h).

The Panel Button De-bounce is an input function. After the panel button de-bounce is enabled, a related status bit will be set when an active low pulse is detected on a GPIO pin. The status bits will be cleared by writing "1" to them. Panel Button De-bounce Interrupt will be issued if any one of the status bit is set. However, the new setting status will not issue another interrupt unless the previous status bit is cleared before being set.

The SMI# is a non-maskable interrupt dedicated to the transparent power management. It consists of different enabled interrupts generated from each of the functional blocks in the IT8705F. The interrupts redirect the

SMI# output via the SMI# Control Register. The SMI# Status Register 1 is used to read the status of the SMI input events. All the SMI# status register bits can be cleared when the corresponding source events become invalidated. These bits can be cleared by writing "1" to themselves. The SMI# event can be programmed as pulse mode or level mode whenever an SMI# event occurs. The logic equation of the SMI# event is described below:

SMI# event = (EN_FIRQ and FIRQ) or (EN_S1IRQ and S1IRQ) or (EN_S2IRQ and S2IRQ) or (EN_PIRQ and PIRQ) or (EN_EC and EC_SMI) or (EN_CIRIRQ or CIRIRQ) or (EN_MIDIIRQ or MIDIIRQ).

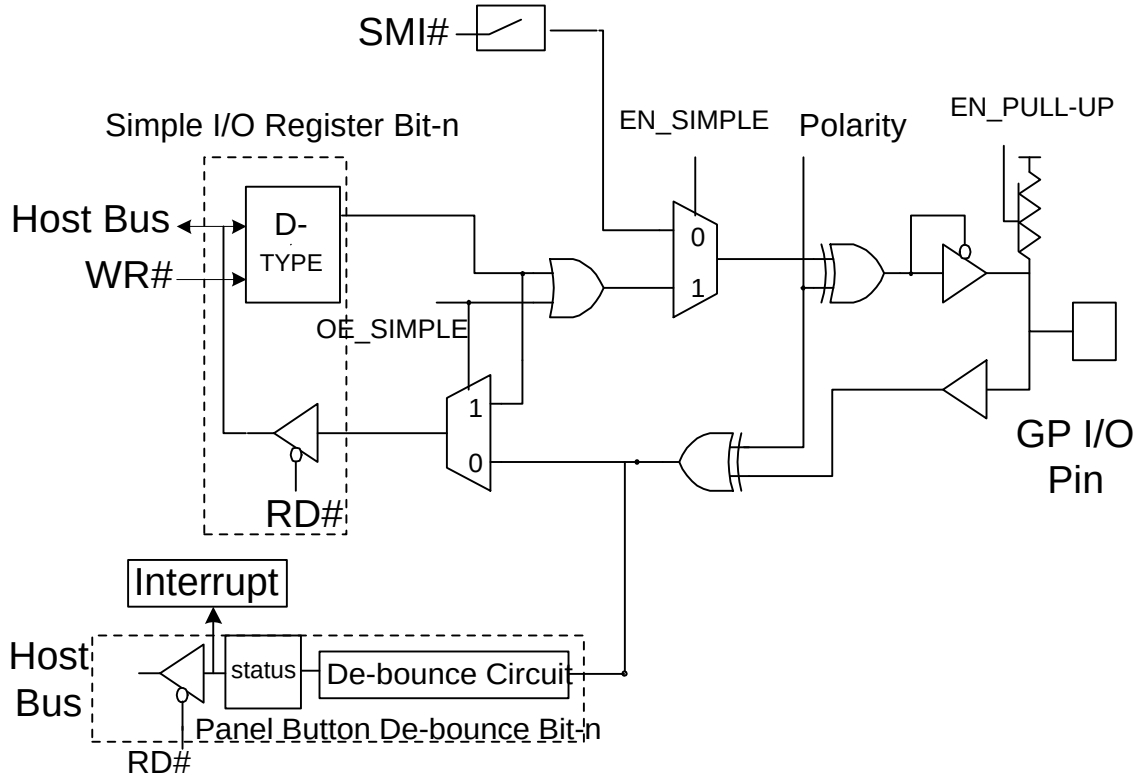


Figure 9-3. General Logic of GPIO Function

9.4 Power Management Event (PME#)

PME# is used to wake up the system from low-power states (S1-S5). There are three types of PME# events: RI1#, RI2# and CIR events. RI1# and RI2# are Ring Indicator of Modem status at ACPI S1 or S2. A falling edge on these pins issues PME# events if the enable bits are set.

A CIR event is generated if the input CIR RX pattern is the same as the previous stored pattern stored at PME Special Code Index and Data Registers (LDN=04h, Index=F5h, and F6h). The total maximum physical codes are nineteen bytes (from Index 20h to 32h). The first byte (Index 20h) is used to specify the pattern length in bytes. Bits[7:0] are used when VCC is ON; and bits[3:0] when VCC goes OFF. The length represented in each 4 bits will be incremented by 3 internally as the actual length to be compared. For most of the CIR protocols, the first several bytes are always the same for each key (or pattern). The differences are always placed in the last several bytes. Thus, the system designer can program the IT8705F to generate a CIR PME# event as any keys when VCC is ON and a special key (i.e. POWER-ON) when VCC power goes OFF.

9.5 Environment Controller (Enhanced Hardware Monitor and Fan Controller)

9.5.1 Overview

The Environment Controller (EC), built in the IT8705F, includes eight voltage inputs, three temperature sensor inputs, three Fan Tachometer inputs, and three sets of advanced Fan Controllers. The EC monitors the hardware environment and executes environmental control for personal computers.

The IT8705F contains an 8-bit ADC (Analog-to-Digital Converter), responsible for monitoring the voltages and temperatures. The ADC converts the analog inputs, ranging from 0V to 4.096V, to 8-bit digital bytes. Thanks to the additional external components, the analog inputs are able to monitor different voltage ranges, in addition to monitoring the fixed input range of 0V to 4.096V. The temperature sensor inputs can be converted to 8-bit digital bytes, and monitor the temperature around the thermistors or thermal diode. A built-in ROM is also provided to adjust the non-linear characteristics of thermistors.

Fan Tachometer inputs are digital inputs with an acceptable range of 0V to 5V, and are responsible for measuring the Fan's tachometer pulse periods. FAN_TAC1 and FAN_TAC2 are equipped with programmable divisors, and can be used to measure different fan speed ranges. FAN_TAC3 is equipped with the fixed divisor, and can only be used in the default range.

The EC of the IT8705F provides multiple internal registers and an interrupt generator for programmers to monitor the environment and control the FANs.

9.5.2 Interfaces

LPC Bus: The Environment Controller of the IT8705F decodes two addresses.

Table 9-1. Address Map on the ISA Bus

Register or Ports	Address
Address register of the EC	Base+05h
Data register of the EC	Base+06h

Note 1. The Base Address is determined by the Logical Device configuration registers of the Environment Controller (LDN=04h, registers index= 60h, 61h).

To access an EC register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

The BUSY bit (bit 7) in the address register (Base+05h) will be set during the ISA driver access. If the BUSY bit is set, it means an ISA driver is accessing, and other drivers are limited to reading the address register (Base+05h) only. These ISA drivers can only access the address register after the BUSY bit is cleared. By checking this bit status before accessing the address register, multiple ISA drivers can access the EC at one time, and are not required to communicate with each other.

9.5.3 Registers

9.5.3.1 Address Port (Base+05h, Default=00h):

Bit	Description
7	**Outstanding; Read only** This bit is set when a data write is performed to Address Port via the ISA bus or when a Serial bus transaction is in progress. This bit can be cleared when the Serial Bus transaction is completed, or when a data write/read is performed to/from the Data Port.
6-0	**Index: Internal Address of RAM and Registers**

Table 9-2. Environment Controller Registers

Index	R/W	Default	Registers or Action
00h	R/W	18h	Configuration
01h	RO	00h	Interrupt Status 1
02h	RO	00h	Interrupt Status 2
03h	RO	00h	Interrupt Status 3
04h	R/W	00h	SMI# Mask 1
05h	R/W	00h	SMI# Mask 2
06h	R/W	00h	SMI# Mask 3
07h	R/W	00h	Interrupt Mask 1
08h	R/W	00h	Interrupt Mask 2
09h	R/W	00h	Interrupt Mask 3
0Ah	RO	-	Reserved register
0Bh	R/W	09h	Fan Tachometer Divisor Register
0Dh	RO	-	Fan Tachometer 1 Reading Register
0Eh	RO	-	Fan Tachometer 2 Reading Register
0Fh	RO	-	Fan Tachometer 3 Reading Register
10h	R/W	-	Fan Tachometer 1 Limit Register
11h	R/W	-	Fan Tachometer 2 Limit Register
12h	R/W	-	Fan Tachometer 3 Limit Register
13h	R/W	00h	Fan Controller Main Control Register
14h	R/W	00h	FAN_CTL Control Register
15h	R/W	00h	FAN_CTL1 PWM Control Register
16h	R/W	00h	FAN_CTL2 PWM Control Register
17h	R/W	00h	FAN_CTL3 PWM Control Register
20h	RO	-	VIN0 Voltage Reading Register
21h	RO	-	VIN1 Voltage Reading Register

Table 9-2. Environment Controller Registers [cont' d]

Index	R/W	Default	Registers or Action
22h	RO	-	VIN2 Voltage Reading Register
23h	RO	-	VIN3 Voltage Reading Register
24h	RO	-	VIN4 Voltage Reading Register
25h	RO	-	VIN5 Voltage Reading Register
26h	RO	-	VIN6 Voltage Reading Register
27h	RO	-	VIN7 Voltage Reading Register
28h	RO	-	VBAT Voltage Reading Register
29h	RO	-	TMPIN1 Temperature Reading Register
2Ah	RO	-	TMPIN2 Temperature Reading Register
2Bh	RO	-	TMPIN3 Temperature Reading Register
30h	R/W	-	VIN0 High Limit Register
31h	R/W	-	VIN0 Low Limit Register
32h	R/W	-	VIN1 High Limit Register
33h	R/W	-	VIN1 Low Limit Register
34h	R/W	-	VIN2 High Limit Register
35h	R/W	-	VIN2 Low Limit Register
36h	R/W	-	VIN3 High Limit Register
37h	R/W	-	VIN3 Low Limit Register
38h	R/W	-	VIN4 High Limit Register
39h	R/W	-	VIN4 Low Limit Register
3Ah	R/W	-	VIN5 High Limit Register
3Bh	R/W	-	VIN5 Low Limit Register
3Ch	R/W	-	VIN6 High Limit Register
3Dh	R/W	-	VIN6 Low Limit Register
3Eh	R/W	-	VIN7 High Limit Register
3Fh	R/W	-	VIN7 Low Limit Register
40h	R/W	-	TMPIN1 High Limit Register
41h	R/W	-	TMPIN1 Low Limit Register
42h	R/W	-	TMPIN2 High Limit Register
43h	R/W	-	TMPIN2 Low Limit Register
44h	R/W	-	TMPIN3 High Limit Register
45h	R/W	-	TMPIN3 Low Limit Register
48h	R/W	2Dh	Reserved
50h	R/W	00h	ADC Voltage Channel Enable Register
51h	R/W	00h	ADC Temperature Channel Enable Register

Table 9-2. Environment Controller Registers [cont'd]

Index	R/W	Default	Registers or Action
52h	R/W	7Fh	Reserved
53h	R/W	7Fh	Reserved
54h	R/W	7Fh	Reserved
58h	RO	90h	ITE Vendor ID Register
59h	R/W	56h	Thermal Diode Zero Degree Adjust Register
5Ch	R/W	00h	Special Control and Beep Event Enable Register
5Dh	R/W	00h	Beep Frequency Divisor of Fan Event Register
5Eh	R/W	00h	Beep Frequency Divisor of Voltage Event Register
5Fh	R/W	00h	Beep Frequency Divisor of Temperature Event Register
60h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of OFF Register
61h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Low Speed Register
62h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Medium Speed Register
63h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of High Speed Register
64h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Over Temperature Limit Register
65h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Low Speed PWM Register
66h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Medium Speed PWM Register
67h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode High Speed PWM Register
68h	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of OFF Register
69h	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Low Speed Register
6Ah	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Medium Speed Register
6Bh	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of High Speed Register
6Ch	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Over Temperature Limit Register
6Dh	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Low Speed PWM Register
6Eh	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Medium Speed PWM Register
6Fh	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode High Speed PWM Register
70h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of OFF Register
71h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Low Speed Register
72h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Medium Speed Register
73h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of High Speed Register
74h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Over Temperature Limit Register
75h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Low Speed PWM Register
76h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Medium Speed PWM Register
77h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode High Speed PWM Register

9.5.3.2 Register Description

9.5.3.2.1 Configuration Register (Index=00h, Default=18h)

Bit	R/W	Description
7	R/W	**Initialization** A "1" restores all registers to their individual default values, except the Serial Bus Address Register. This bit clears itself when the default value is 0.
6	R/W	**Update VBAT Voltage Reading**
5	R/W	**Reserved**
4	RO	**Read Only**, Always "1".
3	R/W	**INT_Clear** A "1" disables the SMI# and IRQ outputs with the contents of interrupt status bits remain unchanged.
2	R/W	**IRQ enables the IRQ Interrupt output**
1	R/W	**SMI# Enable** A "1" enables the SMI# interrupt output.
0	R/W	**Start** A "1" enables the startup of monitoring operations while a "0" sends the monitoring operation in the standby mode.

9.5.3.2.2 Interrupt Status Register 1 (Index=01h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-3	RO	**Reserved**
2-0	RO	A "1" indicates the FAN_TAC3-1 Count limit has been reached.

9.5.3.2.3 Interrupt Status Register 2 (Index=02h, Default=00h)

Reading this register will clear itself after the read operation is completed.

Bit	R/W	Description
7-0	RO	A "1" indicates a High or Low limit of VIN7-0 has been reached.

9.5.3.2.4 Interrupt Status Register 3 (Index=03h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-3	RO	**Reserved**
2-0	RO	A "1" indicates a High or Low limit of Temperature 3-1 has been reached.

9.5.3.2.5 SMI# Mask Register 1 (Index=04h, Default=00h)

Bit	R/W	Description
7-3	R/W	**Reserved**
2-0	R/W	A "1" disables the FAN_TAC3-1 interrupt status bit for SMI#.

9.5.3.2.6 SMI# Mask Register 2 (Index=05h, Default=00h)

Bit	R/W	Description
7-0	R/W	A "1" disables the VIN7-0 interrupt status bit for SMI#.

9.5.3.2.7 SMI# Mask Register 3 (Index=06h, Default=00h)

Bit	R/W	Description
7-3	R/W	**Reserved**
2-0	R/W	A "1" disables the Temperature 3-1 interrupt status bit for SMI#.

9.5.3.2.8 Interrupt Mask Register 1 (Index=07h, Default=00h)

Bit	R/W	Description
7-5	R/W	**Reserved**
4	R/W	A "1" disables the Case Open Intrusion interrupt status bit for IRQ.
3	R/W	**Reserved**
2-0	R/W	A "1" disables the FAN_TAC3-1 interrupt status bit for IRQ.

9.5.3.2.9 Interrupt Mask Register 2 (Index=08h, Default=00h)

Bit	R/W	Description
7-0	R/W	A "1" disables the VIN7-0 interrupt status bit for IRQ.

9.5.3.2.10 Interrupt Mask Register 3 (Index=09h, Default=00h)

Bit	R/W	Description
7-3	R/W	**Reserved**
2-0	R/W	A "1" disables the Temperature 3-1 interrupt status bit for IRQ.

9.5.3.2.11 Fan Tachometer Divisor Register (Index=0Bh, Default=09h)

Bit	R/W	Description
7	-	**Reserved**
6	R/W	**FAN_TAC3 Counter Divisor** 0: divided by 2 1: divided by 8
5-3	R/W	**FAN_TAC2 Counter Divisor** 000: divided by 1 100: divided by 16 001: divided by 2 101: divided by 32 010: divided by 4 110: divided by 64 011: divided by 8 111: divided by 128
2-0	R/W	**FAN_TAC1 Counter Divisor** 000: divided by 1 100: divided by 16 001: divided by 2 101: divided by 32 010: divided by 4 110: divided by 64 011: divided by 8 111: divided by 128

9.5.3.2.12 Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)

Bit	R/W	Description
7-0	RO	**The number of counts of the internal clock per revolution.**

9.5.3.2.13 Fan Tachometer 1-3 Limit Registers (Index=10h-12h)

Bit	R/W	Description
7-0	R/W	**Limit Value**

9.5.3.2.14 Fan Controller Main Control Register (Index=13h, Default=00h)

Bit	R/W	Description
7	RO	**Reserved**
6-4	R/W	**FAN_TAC3-1 Enable**
3	R/W	**Reserved**
2-0	R/W	**FAN_CTL3-1 Output Mode Selection** 0: ON/OFF mode. 1: SmartGuardian mode.

9.5.3.2.15 FAN_CTL Control Register (Index=14h, Default=00h)

Bit	R/W	Description
7	R/W	**Polarity** 0: FAN_CTL3-1 are low active (default). 1: FAN_CTL3-1 are high active.
6-4	R/W	**PWM_CLK** These bits select the step clock of the FAN_CTL PWM mode. 000: 48M (PWM frequency = 48M/128 = 375K) 001: 24M 010: 12M 011: 8M 100: 6M 101: 3M 110: 1.5M 111: 0.75M
3	R/W	**Reserved**
2-0	R/W	**FAN_CTL3-1 ON/OFF Mode Control** These bits are only available when the relative output modes are selected in ON/OFF mode. 0: OFF 1: ON

9.5.3.2.16 FAN_CTL1 PWM Control Register (Index=15h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN_CTL1 PWM mode Automatic/Software Operation Selection** 0: Software operation. 1: Automatic operation.
6-0	R/W	**128 Steps of PWM Control when in Software Operation (bit 7=0), or Temperature Input Selection when in Automatic Operation (bit 7=1).** Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.5.3.2.17 FAN_CTL2 PWM Control Register (Index=16h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN_CTL2 PWM mode Automatic/Software Operation Selection.** 0: Software operation. 1: Automatic operation.
6-0	R/W	**128 steps of PWM Control When in Software Operation (bit 7=0), or Temperature Input Selection When in Automatic Operation (bit 7=1).** Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.5.3.2.18 FAN_CTL3 PWM Control Register (Index=17h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN_CTL3 PWM Mode Automatic/Software Operation Selection.** 0: Software operation. 1: Automatic operation.
6-0	R/W	**128 Steps PWM Control When in Software Operation (bit 7=0), or Temperature Input Selection When in Automatic Operation (bit 7=1).** Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.5.3.2.19 VIN7-VIN0 Voltage Reading Registers (Index=27h-20h)

Bit	R/W	Description
7-0	R/W	**Voltage Reading Value**

9.5.3.2.20 VBAT Voltage Reading Register (Index=28h)

Bit	R/W	Description
7-0	R/W	**VBAT Voltage Reading Value**

9.5.3.2.21 TMPIN3-1 Temperature Reading Registers (Index=2Bh-29h)

Bit	R/W	Description
7-0	R/W	**Temperature Reading Value**

9.5.3.2.22 VIN7-0 High Limit Registers (Index=3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h and 30h)

Bit	R/W	Description
7-0	R/W	**High Limit Value**

9.5.3.2.23 VIN7-0 Low Limit Registers (Index=3Fh, 3Dh, 3Bh, 39h, 37h, 35h, 33h and 31h)

Bit	R/W	Description
7-0	R/W	**Low Limit Value**

9.5.3.2.24 TMPIN3-1 High Limit Registers (Index=44h, 42h and 40h)

Bit	R/W	Description
7-0	R/W	**High Limit Value**

9.5.3.2.25 TMPIN3-1 Low Limit Registers (Index=45h, 43h and 41h)

Bit	R/W	Description
7-0	R/W	**Low Limit Value**

9.5.3.2.26 Reserved Register (Index=48h, Default=2Dh)

9.5.3.2.27 ADC Voltage Channel Enable Register (Index=50h, Default=00h)

Bit	R/W	Description
7-0	R/W	**ADC VIN7-VIN0 Scan Enable**

9.5.3.2.28 ADC Temperature Channel Enable Register (Index=51h, Default=00h)

TMPIN3-1 cannot be enabled in both Thermal Register mode and Thermal Diode (Diode connected Transistor) mode.

Bit	R/W	Description
7-6	R/W	**Reserved**
5-3	R/W	**TMPIN3-1 are enabled in Thermal Resistor mode**
2-0	R/W	**TMPIN3-1 are enabled in Thermal Diode (or Diode-connected Transistor) mode**

9.5.3.2.29 Reserved Registers (Index=54h-52h, Default=7Fh)

9.5.3.2.30 Vendor ID Register (Index=58h, Default=90h)

Bit	R/W	Description
7-0	RO	**ITE Vendor ID. Read Only.**

9.5.3.2.31 Thermal Diode Zero Degree Adjust Register (Index=59h, Default=56h)

This register is read-only unless the bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	**Thermal Diode Zero Degree Voltage Value (default: 0.664V 156h)**

9.5.3.2.32 Special Control and Beep Event Enable Register (Index=5Ch, Default=00h)

The individual channel selections of each event are the same with SMI mask registers.

Bit	R/W	Description
7	R/W	**Thermal Diode Zero Degree Adjust Register Write Enable**
6-3	R/W	**Reserved**
2	R/W	**Temperature Event of SMI to generate Beep Enable** 0: Disable Temperature event to generate Beep (default). 1: Enable Temperature event to generate Beep.
1	R/W	**Voltage Event of SMI to generate Beep Enable** 0: Disable Voltage event to generate Beep (default). 1: Enable Voltage event to generate Beep.
0	R/W	**FAN Event of SMI to generate Beep Enable** 0: Disable FAN event to generate Beep (default). 1: Enable FAN event to generate Beep.

9.5.3.2.33 Beep Frequency Divisor of Fan Event Register (Index=5Dh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor** Beep Tone = 500 / (bit[7:4]+1).
3-0	R/W	**Frequency Divisor** Beep frequency = 10K / (bit[3:0]+1).

9.5.3.2.34 Beep Frequency Divisor of Voltage Event Register (Index=5Eh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor** Beep Tone = 500 / (bit[7:4]+1).
3-0	R/W	**Frequency Divisor** Beep frequency = 10K / (bit[3:0]+1).

9.5.3.2.35 Beep Frequency Divisor of Temperature Event Register (Index=5Fh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor** Beep Tone = 500 / (bit[7:4]+1).
3-0	R/W	**Frequency Divisor** Beep frequency = 10K / (bit[3:0]+1).

9.5.3.2.36 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of OFF Registers (Index=70h, 68h, 60h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan OFF**

9.5.3.2.37 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Low Speed Registers (Index=71h, 69h and 61h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan Low Speed**

9.5.3.2.38 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Medium Speed Registers (Index=72h, 6Ah and 62h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan Medium Speed**

9.5.3.2.39 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of High Speed Registers (Index=73h, 6Bh and 63h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan High Speed**

9.5.3.2.40 FAN_CTL3-1 SmartGuardian Automatic Mode Over Temperature Limit Registers (Index=74h, 6Ch and 64h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Over Temperature Limit Value**

9.5.3.2.41 FAN_CTL3-1 SmartGuardian Automatic Mode Low Speed PWM Registers (Index=75h, 6Dh and 65h, Default=00h)

Bit	R/W	Description
7	R/W	**Reserved**
6-0	R/W	**PWM Value of Fan Low Speed**

9.5.3.2.42 FAN_CTL3-1 SmartGuardian Automatic Mode Medium Speed PWM Registers (Index=76h, 6Eh and 66h, Default=00h)

Bit	R/W	Description
7	R/W	**Reserved**
6-0	R/W	**PWM Value of Fan Medium Speed**

9.5.3.2.43 FAN_CTL3-1 SmartGuardian Automatic Mode High Speed PWM Registers (Index=77h, 6Fh and 67h, Default=00h)

Bit	R/W	Description
7	R/W	**Reserved**
6-0	R/W	**PWM Value of Fan High Speed**

9.5.4 Operation

9.5.4.1 Power On RESET and Software RESET

When the system power is first applied, the EC performs a "power on reset" on the registers, which will return to the default values due to system hardware reset. The ADC will be temporarily active to read the VBAT pin and then goes inactive. There is a software reset (bit 7 of Configuration register) that can accomplish all the functions as the hardware reset does.

9.5.4.2 Starting Conversion

The monitoring function in the EC is activated when bit 3 of Configuration Register is cleared (low) and bit 0 of Configuration Register is set (high). Otherwise, several enable bits should be set to enable the monitoring function. Those enable bits are categorized into three groups: voltages, temperatures and Fan tachometers. Before the EC monitoring function can be used, the steps below should be followed:

1. Set the limit
2. Set the Interrupt Masks
3. Set the Enable bits

The EC monitoring process can then begin.

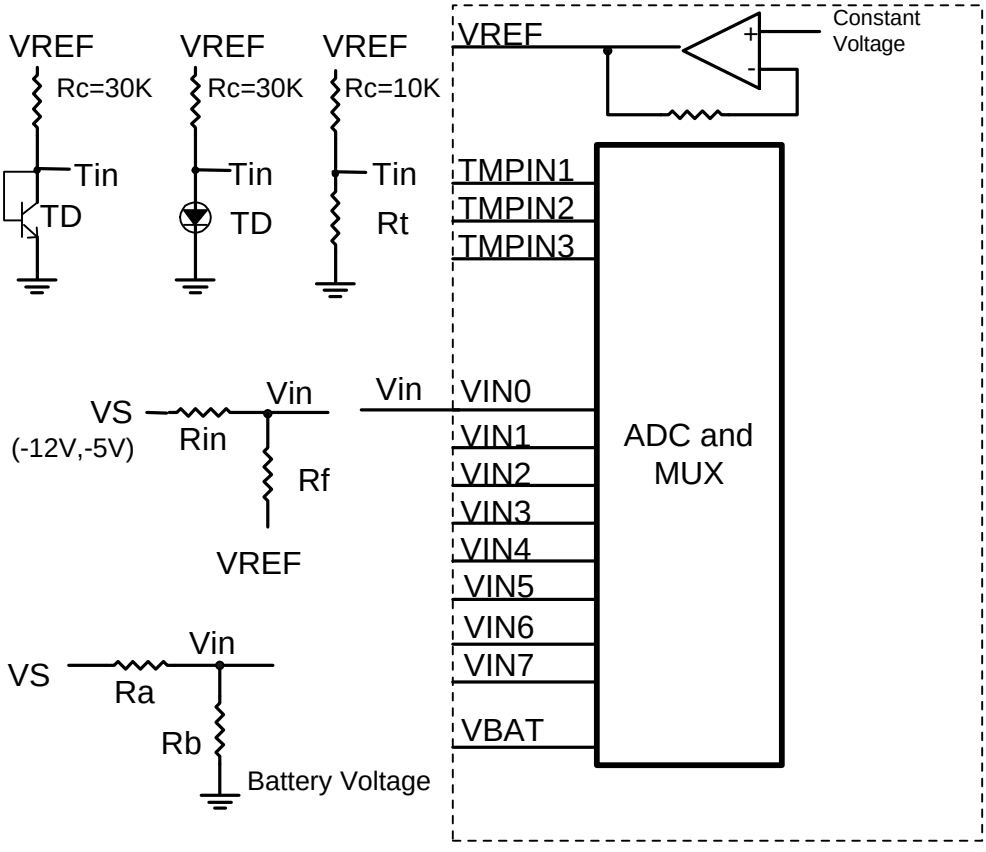


Figure 9-4. Application Example Resistor should provide approximately 2V at the Analog Inputs

9.5.4.3 Voltage and Temperature Input

The 8-bit ADC has a 16mV LSB, with a 0V to 4.096V input range. The 2.5V and 3.3V supplies of PC applications can be directly connected to the inputs. The 5V and 12V inputs should be divided into the acceptable range. When the divided circuit is used to measure the positive voltage, the recommended range for Ra and Rb is from 10KΩ to 100KΩ. The negative voltage can be measured by the same divider when the divider is connected to VREF (constant voltage, 4.096V), rather than ground. The temperature measurement system of the EC converts the voltage of the TMPINs to 8-bit two' s-complement. The system also includes an OP amp providing a constant voltage. It also additionally includes an external thermistor, a constant resistance, the ADC and a conversion table ROM.

Temperature	Digital Output Format	
	Binary	Hex
+ 125°C	01111101	7Dh
+ 25°C	00011001	19h
+ 1°C	00000001	01h
+ 0°C	00000000	00h
- 1°C	11111111	FFh
- 25°C	11100111	E7h
- 55°C	11001001	C9h

With the addition of the external application circuit, the actual voltages are calculated as below:

Positive Voltage: Vs = Vin X (Ra+Rb) / Rb
Negative Voltage: Vs = (1+Rin/Rf) x Vin - (Rin/Rf) x VREF

All the analog inputs are equipped with the internal diodes that clamp the input voltage exceeding the power supply and ground. But, the limiting input current resistor is recommended when no dividing circuit is available.

9.5.4.4 Layout and Grounding

A separate and low-impedance ground plane for analog ground is needed in achieving accurate measurement. The analog ground also provides a ground point for the voltage dividers including the temperature loops and analog components. Analog components such as voltage dividers, feedback resistors and the constant resistors of the temperature loops should be located as close as possible to the IT8705F. But, the thermistors of the temperature loops should be positioned within the measured area. In addition, the power supply bypass, and the parallel combination of 10µF and 0.1µF bypass capacitors connected between VCC and analog ground, should also be located as close as possible to the IT8705F.

Due to the small differential voltage of thermal diode (diode-connected transistor), PCB layout recommendations are listed below:

- Position the sensor as close as possible
- Ground of the sensor should be directly short to GNDA with excellent noise immunity
- Keep trace away from the noise source. (High voltage, fast data bus, fast clock , CRTs ..)
- Wider trace width (10mil at least) and guard ground (flanking and under) are recommended
- Position the 0.1µF bypass capacitors as close to the IT8705F as possible

9.5.4.5 Fan Tachometer

The Fan Tachometers gate a 22.5 kHz clock into an 8-bit counter (maximum count=255) for one period of the input signals. Several divisors, located in Fan Divisor Register, are provided for FAN_TAC1 and FAN_TAC2, and are used to modify the monitoring range. FAN_TAC3 is not adjustable, and its divisor value is always set to 2. Counts are based on 2 pulses per resolution tachometer output.

RPM = 1.35 X 10^6 / (Count X Divisor)

The maximum input signal range is from 0 to VCC. The additional application is needed to clamp the input voltage and current.

9.5.4.6 Interrupt of the EC

The EC generates the Interrupts when the Limit registers of the analog voltage, temperature, and Fan monitor are exceeded.

All the interrupts are indicated in two Interrupt Status Registers. The IRQ and SMI# outputs have individual mask registers. These two Interrupts can also be enabled/disabled in the Configuration Register. The Interrupt Status Registers will be reset after being read. When the Interrupt Status Registers are cleared, the Interrupt lines will also be cleared. When a read operation is completed before the completion of the monitoring loop sequence, it indicates an Interrupt Status Register has been cleared. Due to slow monitoring sequence, the EC needs 1.5 seconds to allow all the EC registers to be safely updated between completed read operations. When bit 3 of the Configuration Register is set to high, the Interrupt lines are cleared and the monitoring loop will be stopped. The loop will resume when this bit is cleared.

All the analog voltage inputs have high and low Limit Registers that generate Interrupts, except that the Fan monitoring inputs only have low Limit Register to warn the host.

The IT8705F provides two modes dedicated to temperature interrupts in the EC: “Interrupt” mode and “Comparator” mode. In “Interrupt” mode, an interrupt will be generated whenever the temperature exceeds Th limit, and the corresponding Interrupt status bits will be set to high until being reset by reading Interrupt Status Register 3. Once an interrupt event has occurred by crossing Th limit, then after being reset, an interrupt will only occur again when the temperature goes below TL limit. Again, it will set the corresponding status bit to high until being reset by reading the Interrupt Status Register 3.

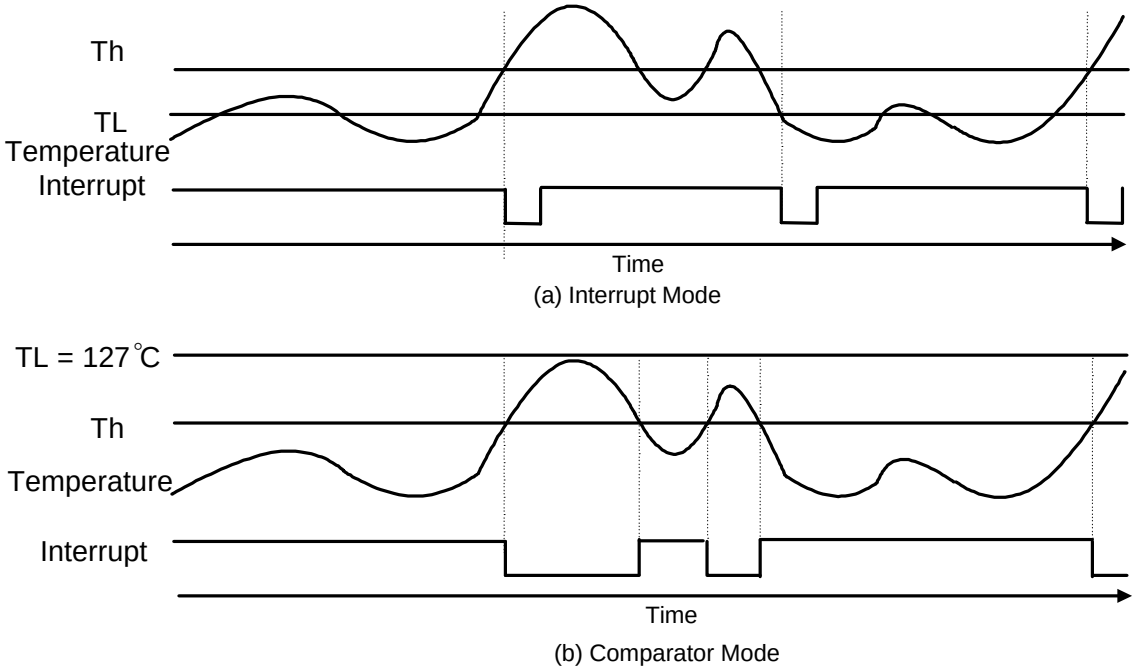


Figure 9-5. Temperature Interrupt Response Diagram

When the TL limit register is set to 127°C, the temperature interrupts enter the **"Comparator" mode**. In this mode, an interrupt will be generated whenever the temperature exceeds the Th limit. The interrupt will also be cleared by reading the Interrupt Status Register 3, but the interrupt will be set again following the completion of another measurement cycle. It will remain set until the temperature goes below the Th limit.

9.5.4.7 Fan Controller FAN_CTL's ON-OFF and SmartGuardian Modes

The IT8705F provides advanced Fan Controllers. Two modes are provided for each controller: ON_OFF and SmartGuardian modes. The former is a logical ON or OFF, and the latter is a PWM output. With the addition of external application, the Fan's voltage values can be varied easily. There are also two mode options in the SmartGuardian mode: software and automatic modes. In the software mode, the PWM value is subject to the changes in the values of bits 6-0 of FAN_CTL PWM Control Registers (Index=15h, 16h, 17h). With the application circuit, FAN_CTL can generate 128 steps of voltage. So, they can vary the voltage by changing the PWM value. Fan speed or other voltage cooling control devices can be varied in 128 steps.

In the Automatic mode, the PWM value is subject to the specific temperature inputs by five stages (OFF, Low Level, Medium Level, High Level and Full On). The PWM values of the Low, Medium and High Levels are pre-loaded. Each of Fan's control sources (temperature inputs) can be any of the three temperature inputs, and are determined by bits 1-0 of FAN_CTL PWM Control Registers (Index=15h, 16h, 17h). When the source temperature is below the Low Temperature (Index=71h, 69h, 61h), the FAN_CTL output will enter OFF state. When the temperature is between Low and Medium Temperature (Index=72h, 6Ah, 62h), the output will perform Low Level PWM; Medium Level PWM when between Medium and High Temperature (Index =73h, 6Bh, 63h); High Level PWM when between the High and Over Temperature (Index=74h, 6Ch, 64h). When any of the Over Temperatures is exceeded, all the FAN_CTL outputs will be Full ON. The FAN_CTL output will not return to the OFF state until the source temperature goes below the OFF Temperature limit (Index=70h, 68h, 60h).

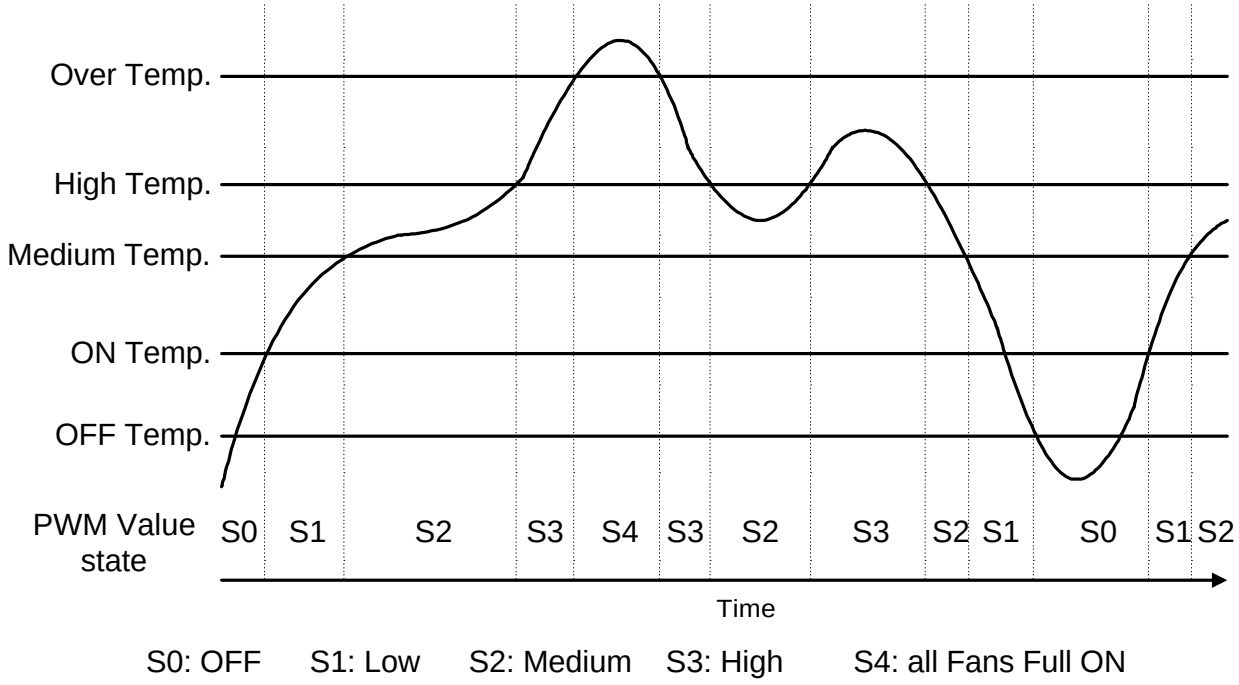


Figure 9-6. SmartGuardian Automatic Mode

9.6 Floppy Disk Controller (FDC)

9.6.1 Introduction

The Floppy Disk Controller provides the interface between a host processor and up to two floppy disk drives. It integrates a controller and a digital data separator with write precompensation, data rate selection logic, microprocessor interface, and a set of registers.

The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in PC/AT mode and supports 3-mode type drives. Additionally, the FDC is software compatible with the 82077.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD.

The controller manages data transfers using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution, and Result. Not all commands utilize all these three phases.

9.6.2 Reset

The IT8705F device implements both software and hardware reset options for the FDC. Either type of the resets will reset the FDC, terminating all operations and placing the FDC into an idle state. A reset during a write to the disk will corrupt the data and the corresponding CRC.

9.6.3 Hardware Reset (LRESET# Pin)

When the FDC receives a LRESET# signal, all registers of the FDC core are cleared (except those programmed by the SPECIFY command). To exit the reset state, the host must clear the DOR bit.

9.6.4 Software Reset (DOR Reset and DSR Reset)

When the reset bit in the DOR or the DSR is set, all registers of the FDC core are cleared. A reset performed by setting the reset bit in the DOR has higher priority over a reset performed by setting the reset bit in the DSR. In addition, to exit the reset state, the DSR bit is self-clearing, while the host must clear the DOR bit.

9.6.5 Digital Data Separator

The internal digital data separator is comprised of a digital PLL and associated support circuitry. It is responsible for synchronizing the raw data signal read from the floppy disk drive. The synchronized signal is used to separate the encoded clock from the data pulses.

9.6.6 Write Precompensation

Write precompensation is a method that can be used to adjust the effects of bit shift on data as it is written to the disk. It is harder for the data separator to read data that has been subject to bit shifting. Soft read errors can occur due to such bit shifting. Write precompensation predicts where the bit shifting might occur within a data pattern and shifts the individual data bits back to their nominal positions. The FDC permits the selections of write precompensation via the Data Rate Select Register (DSR) bits 2 through 4.

9.6.7 Data Rate Selection

Selecting one of the four possible data rates for the attached floppy disks is accomplished by setting the Diskette Control Register (DCR) or Data Rate Select Register (DSR) bits to 0 and 1. The data rate is determined by the last value that is written to either the DCR or the DSR. When the data rate is set, the data separator clock is scaled appropriately.

9.6.8 Status, Data and Control Registers

9.6.8.1 Digital Output Register (DOR, FDC Base Address + 02h)

This is a **read/write** register. It controls drive selection and motor enables as well as a software reset bit and DMA enable. The I/O interface reset may be used at any time to clear the DOR's contents.

Table 9-3. Digital Output Register (DOR)

Bit	Symbol	R/W	Description
7-6	-	-	**Reserved**
5	MOTB EN	R/W	**Drive B Motor Enable** 0: Disable Drive B Motor. 1: Enable Drive B Motor.
4	MOTA EN	R/W	**Drive A Motor Enable** 0: Disable Drive A Motor. 1: Enable Drive A Motor.
3	DMAEN	R/W	**Disk Interrupt and DMA Enable** 0: Disable disk interrupt and DMA (DRQx, DACKx#, TC and INTx). 1: Enable disk interrupt and DMA.
2	RESET#	R/W	**FDC Function Reset** 0: Reset FDC Function. 1: Clear Reset of FDC Function. This reset does not affect the DSR, DCR or DOR.
1	-	-	**Reserved**
0	DVSEL	R/W	**Drive Selection** 0: Select Drive A. 1: Select Drive B.

9.6.8.2 Tape Drive Register (TDR, FDC Base Address + 03h)

This is a **read/write** register and is included for 82077 software compatibility. The contents of this register are not used internal to the device.

Table 9-4. Tape Drive Register (TDR)

Bit	Symbol	R/W	Description
7-2	-	-	**Undefined**
1-0	TP_SEL [1:0]	R/W	**Tape Drive Selection** TP_SEL[1:0] : Drive selected 00: None 01: 1 10: 2 11: 3

9.6.8.3 Main Status Register (MSR, FDC Base Address + 04h)

This is a **read only** register. It indicates the general status of the FDC, and is able to receive data from the host. The MSR should be read before each byte is sent to or received from the Data register, except when in DMA mode.

Table 9-5. Main Status Register (MSR)

Bit	Symbol	R/W	Description
7	RQM	RO	**FDC Request for Master** 0: The FDC is busy and cannot receive data from the host. 1: The FDC is ready and the host can transfer data.
6	DIO	RO	**Data I/O Direction** Indicate the direction of data transfer once a RQM has been set 0: Write. 1: Read.
5	NDM	RO	**Non-DMA Mode** This bit selects Non-DMA mode of operation 0: DMA mode selected. 1: Non-DMA mode selected. This mode is selected via the SPECIFY command during the Execution phase of a command.
4	CB	RO	**Diskette Control Busy** Indicate a command is in progress (the FDD is busy) 0: A command has been executed and the end of the Result phase has been reached. 1: A command is being executed.
3-2	-	-	**Reserved**
1	DBB	RO	**Drive B Busy** Indicate Whether Drive B is in the SEEK portion of a command 0: Not busy. 1: Busy.
0	DAB	RO	**Drive A Busy** Indicate Whether Drive A is in the SEEK portion of a command 0: Not busy. 1: Busy.

9.6.8.4 Data Rate Select Register (DSR, FDC Base Address + 04h)

This is a **write only** register. It is used to determine the data rate, amount of write precompensation, power down mode, and software reset. The data rate of the floppy controller is the most recent write of either the DSR or DCR. The DSR is unaffected by a software reset. The DSR can be set to 02h by a hardware reset, and the “02h” represents the default precompensation, and 250 Kbps in data transfer rate.

Table 9-6. Data Rate Select Register (DSR)

<table>
<tr><th>Bit</th><th>Symbol</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>S/W RESET</td><td>WO</td><td>Software Reset
Software Reset. It is active high and shares the same function with the RESET# of the DOR except that this bit is self-clearing.</td></tr>
<tr><td>6</td><td>POWER DOWN</td><td>WO</td><td>Power Down
When this bit is written with a “1”, the floppy controller is put into manual low power mode. The clocks of the floppy controller and data separator circuits will be turned off until a software reset or the Data Register or Main Status Register is accessed.</td></tr>
<tr><td>5</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>4-2</td><td>PRE-COMP 2-0</td><td>WO</td><td>Precompensation Select
These three bits are used to determine the value of write precompensation that will be applied to the WDATA# pin. Track 0 is the default starting track number, which can be changed by the CONFIGURE command for precompensation.
<table>
<tr><th>PRE_COMP</th><th>Precompensation Delay</th></tr>
<tr><td>111</td><td>0.0 ns</td></tr>
<tr><td>001</td><td>41.7 ns</td></tr>
<tr><td>010</td><td>83.3 ns</td></tr>
<tr><td>011</td><td>125.0 ns</td></tr>
<tr><td>100</td><td>166.7 ns</td></tr>
<tr><td>101</td><td>208.3 ns</td></tr>
<tr><td>110</td><td>250.0 ns</td></tr>
<tr><td>000</td><td>Default</td></tr>
</table>
Default Precompensation Delays
<table>
<tr><th>Data Rate</th><th>Precompensation Delay</th></tr>
<tr><td>1 Mbps</td><td>41.7 ns</td></tr>
<tr><td>500 Kbps</td><td>125.0 ns</td></tr>
<tr><td>300 Kbps</td><td>125.0 ns</td></tr>
<tr><td>250 Kbps</td><td>125.0 ns</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>DRATE1-0</td><td>WO</td><td>Data Rate Select
<table>
<tr><th>Bits 1-0</th><th>Data Transfer Rate</th></tr>
<tr><td>00</td><td>500 Kbps</td></tr>
<tr><td>01</td><td>300 Kbps</td></tr>
<tr><td>10</td><td>250 Kbps (default)</td></tr>
<tr><td>11</td><td>1 Mbps</td></tr>
</table></td></tr>
</table>

9.6.8.5 Data Register (FIFO, FDC Base Address + 05h)

This is an 8-bit **read/write** register. It transfers command information, diskette drive status information, and the result phase status between the host and the FDC. The FIFO consists of several registers in a stack, and only one register in the stack is permitted to transfer information or status to the data bus at a time.

Table 9-7. Data Register (FIFO)

Bit	Symbol	R/W	Description
7-0		R/W	**Data** Command information, diskette drive status, or Result phase status data.

9.6.8.6 Digital Input Register (DIR, FDC Base Address + 07h)

This is a **read only** register and shares this address with the Diskette Control Register (DCR).

Table 9-8. Digital Input Register (DIR)

Bit	Symbol	R/W	Description
7	DSKCHG	RO	**Diskette Change** Indicate the inverting value of the bit monitored from the input of the Floppy Disk Change pin (DSKCHG#).
6-0	-	-	**Undefined**

9.6.8.7 Diskette Control Register (DCR, FDC Base Address + 07h)

This is a **write only** register and shares this address with the Digital Input Register (DIR). The DCR register controls the data transfer rate for the FDC.

Table 9-9. Diskette Control Register (DCR)

Bit	Symbol	R/W	Description
7-2	-	-	**Reserved** Always 0.
1-0	DRATE1-0	WO	**Data Rate Select** **Bits 1-0** **Data Transfer Rate** 00 500 Kbps 01 300 Kbps 10 250 Kbps 11 1 Mbps

9.6.9 Controller Phases

The FDC handles data transfers and control commands in three phases: Command, Execution and Result. Not all commands utilize all these three phases.

9.6.9.1 Command Phase

Upon reset, the FDC enters the Command phase and is ready to receive commands from the host. The host must verify that MSR bit 7 (RQM) = 1 and MSR bit 6 (DIO) = 0, indicating the FDC is ready to receive data. For each command, a defined set of command codes and parameter bytes must be transferred to the FDC in a given order. See sections 9.6.11 and 9.6.12 for details on the various commands. RQM is set false (0) after each byte read cycle, and set true (1) when a new parameter byte is required. The Command phase is completed when this set of bytes has been received by the FDC. The FDC automatically enters the next controller phase and the FIFO is disabled.

9.6.9.2 Execution Phase

Upon the completion of the Command phase, the FDC enters the Execution phase. It is in this phase that all data transfers occur between the host and the FDC. The SPECIFY command indicates whether this data transfer occurs in DMA or non-DMA mode. Each data byte is transferred via an IRQx or DRQx# based upon the DMA mode. On reset, the CONFIGURE command can automatically enable or disable the FIFO. The Execution phase is completed when all data bytes have been received. If the command executed does not require a Result phase, the FDC is ready to receive the next command.

9.6.9.3 Result Phase

For commands that require data written to the FIFO, the FDC enters the Result phase when the IRQ or DRQ is activated. The MSR bit 7 (RQM) and MSR bit 6 (DIO) must equal to 1 to read the data bytes. The Result phase is completed when the host has read each of the defined set of result bytes for the given command. Right after the completion of the phase, RQM is set to 1, DIO is set to 0, and the MSR bit 4 (CB) is cleared, indicating the FDC is ready to receive the next command.

9.6.9.4 Result Phase Status Registers

For commands that contain a Result phase, these **read only** registers indicate the status of the most recently executed command.

Table 9-10. Status Register 0 (ST0)

Bit	Symbol	R/W	Description
7-6	IC	RO	**Interrupt Code** 00: Execution of the command has been completed correctly 01: Execution of the command began, but failed to complete successfully 10: INVALID command 11: Execution of the command was not completed correctly, due to a polling error
5	SE	RO	**Seek End** The FDC executed a SEEK or RE-CALIBRATE command.
4	EC	RO	**Equipment Check** The TRK0# pin was not set after a RE-CALIBRATE command was issued.
3	NU	RO	**Not Used**
2	H	RO	**Head Address** The current head address.
1	DSB	RO	**Drive B selected** Drive B selected.
0	DSA	RO	**Drive A selected** Drive A selected.

Table 9-11. Status Register 1 (ST1)

Bit	Symbol	R/W	Description
7	EN	RO	**End of Cylinder** Indicate the FDC attempted to access a sector beyond the final sector of the track. This bit will be set if the Terminal Count (TC) signal is not issued after a READ DATA or WRITE DATA command.
6	-	-	**Unused.** Always "0".
5	DE	RO	**Data Error** A CRC error occurred in either the ID field or the data field of a sector.
4	OR	RO	**Overrun/ Underrun** An overrun on a READ operation or underrun on a WRITE operation occurs when the FDC is not serviced by the CPU or DMA within the required time interval.
3	-	-	**Reserved.** Always "0".
2	ND	RO	**No Data** No data is available to the FDC when either of the following conditions is met: The floppy disk cannot find the indicated sector while the READ DATA or READ DELETED DATA commands are executed While executing a READ ID command, an error occurs upon reading the ID field while executing a READ A TRACK command, the FDC cannot find the starting sector
1	NW	RO	**Not Writeable** Set when a WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK command is being executed on a write-protected diskette.
0	MA	RO	**Missing Address Mark** This flag bit is set when either of the following conditions is met: The FDC cannot find a Data Address Mark or a Deleted Data Address Mark on the specified track The FDC cannot find any ID address on the specified track after two index pulses are detected from the INDEX# pin

Table 9-12. Status Register 2 (ST2)

Bit	Symbol	R/W	Description
7	-	-	**Unused.** Always "0".
6	CM	RO	**Control Mark** This flag bit is set when either of the following conditions is met: 1. The FDC finds a Deleted Data Address Mark during a READ DATA command 2. The FDC finds a Data Address Mark during a READ DELETED DATA command
5	DD	RO	**Data Error in Data Field** This flag bit is set when a CRC error is found in the data field.
4	WC	RO	**Wrong Cylinder** This flag bit is set when the track address in the ID field is different from the track address specified in the FDC.
3	SH	RO	**Scan Equal Hit** This flag bit is set when the condition of "equal" is satisfied during a SCAN command.
2	SN	RO	**Scan Not Satisfied** This flag bit is set when the FDC cannot find a sector on the cylinder during a SCAN command.
1	BC	RO	**Bad Cylinder** This flag bit is set when the track address equals "FFh" and is different from the track address in the FDC.
0	MD	RO	**Missing Data Address Mark** This flag bit is set when the FDC cannot find a Data Address Mark or Deleted Data Address Mark.

Table 9-13. Status Register 3 (ST3)

Bit	Symbol	R/W	Description
7	FT	RO	**Fault** Indicate the current status of the Fault signal from the FDD.
6	WP	RO	**Write Protect** Indicate the current status of the Write Protect signal from the FDD.
5	RDY	RO	**Ready** Indicate the current status of the Ready signal from the FDD.
4	TK0	RO	**Track 0** Indicate the current status of the Track 0 signal from the FDD.
3	TS	RO	**Two Side** Indicate the current status of the Two Side signal from the FDD.
2	HD	RO	**Head Address** Indicate the current status of the Head Select signal to the FDD.
1-0	US1, US0	RO	**Unit Select** Indicate the current status of the Unit Select signals to the FDD.

9.6.10 Command Set

The FDC utilizes a defined set of commands to communicate with the host. Each command is comprised of a unique first byte, which contains the op-code, and a series of additional bytes, which contain the required set of parameters and results. The op-code byte indicates to the FDC how many additional bytes should be expected for the command being written. The descriptions use a common set of parameter byte symbols, which are presented in Table 9-14. The FDC commands may be executed whenever the FDC is in the Command phase. The FDC checks to see that the first byte is a valid command and, if so, proceeds. An interrupt is issued if it is not a valid command.

Table 9-14. Command Set Symbol Descriptions

Symbol	Name	Description
C	Cylinder Number	The current/selected cylinder (track) number: 0 – 255.
D	Data	The data pattern to be written into a sector.
DC3–DC0	Drive Configuration Bit3-0	Designate which drives are perpendicular drives on the PERPENDICULAR MODE command.
DIR	Direction Control	**Read/write** Head Step Direction Control. 0 = Step Out; 1 = Step In.
DR0, DR1	Disk Drive Select	The selected drive number: 0 or 1.
DTL	Data Length	When N is defined as 00h, DTL designates the number of data bytes which users are going to read out or write into the Sector. When N is not 00h, DTL is undefined.
DFIFO	Disable FIFO	A "1" will disable the FIFO (default). A "0" will enable the FIFO.
EC	Enable Count	If EC=1, DTL of VERIFY command will be SC.
EIS	Enable Implied Seek	If EIS=1, a SEEK operation will be performed before executing any READ or WRITE command that requires the C parameter.
EOT	End of Track	The final sector number on a cylinder. During a READ or WRITE operation, the FDC stops data transfer after the sector number is equal to EOT.
GAP2	Gap 2 Length	By PERPENDICULAR MODE command, this parameter changes Gap 2 length in the format.
GPL	Gap Length	The length of Gap 3. During a FORMAT command, it determines the size of Gap 3.
H	Head Address	The Head number 0 or 1, as specified in the sector ID field. (H = HD in all command words.)
HD	Head	The selected Head number 0 or 1. It also controls the polarity of HDSEL#. (H = HD in all command words.)
HLT	Head Load Time	The Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The Head Unload Time after a READ or WRITE operation has been executed (16 to 240 ms in 16 ms increments).
LOCK		If LOCK=1, DFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command will not be affected by a software reset. If LOCK=0 (default), the above parameters will be set to their default values following a software reset.

Table 9-14. Command Set Symbol Descriptions [cont'd]

Symbol	Name	Description
MFM	FM or MFM Mode	If MFM is low, FM Mode (single density) is selected. If MFM is high, MFM Mode (double density) is selected.
MT	Multi-Track	If MT is high, a Multi-Track operation is to be performed. In this mode, the FDC will automatically start searching for sector 1 on side 1 after finishing a READ/WRITE operation on the last sector on side 0.
N	Number	The number of data bytes written into a sector, where: 00 :128 bytes (PC standard) 01 :256 bytes 02 :512 bytes … 07 :16 Kbytes
NCN	New Cylinder Number	A new cylinder number, which is to be reached as a result of the SEEK operation. Desired position of Head.
ND	Non-DMA Mode	When ND is high, the FDC operates in the non-DMA Mode.
OW	Overwrite	If OW=1, DC3-0 of the PERPENDICULAR MODE command can be modified. Otherwise, those bits cannot be changed.
PCN	Present Cylinder Number	The cylinder number at the completion of a SENSE INTERRUPT STATUS command. Position of Head at present time.
POLLD	Polling Disable	If POLLD=1, the internal polling routine is disabled.
PRETRK	Precompensation Starting Track Number	Programmable from track 0 –255.
R	Record	The sector number, which will be read or written.
RCN	Relative Cylinder Number	To determine the related cylinder offset from present cylinder as used by the RELATIVE SEEK command.
SC		The number of sectors per cylinder.
SK	Skip	If SK=1, the Read Data operation will skip sectors with a Deleted Data Address Mark. Or, the Read Deleted Data operation only accesses sectors with a Deleted Data Address Mark.
SRT	Step Rate Time	The Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives (F=1 ms, E=2 ms, etc.).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0–3 stand for one of four registers that store the status information after a command has been executed. This information is available during the Result phase after command execution. These registers should not be confused with the Main Status Register (selected by A_0 = 0). ST0–3 may be **read only** after a command has been executed and contain information associated with that particular command.
STP		If STP = 1 during a SCAN operation, the data in contiguous sectors are compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.

Table 9-15. Command Set Summary

READ DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	MT	MFM	SK	0	0	1	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution.
	RO	H								
	RO	R								
	RO	N								

READ DELETED DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	MT	MFM	SK	0	1	1	0	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution.
	RO	H								
	RO	R								
	RO	N								

READ A TRACK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	0	0	0	0	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and main system cylinder's contents from index hole to EOT.
Result	RO	ST0								Sector ID information before the command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

WRITE DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	0	0	0	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

WRITE DELETED DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	0	0	1	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

FORMAT A TRACK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	MFM	0	0	1	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	N								Bytes/Sector
	WO	SC								Sectors/Cylinder
	WO	GPL								Gap 3
	WO	D								Filler Byte
Execution	WO	C								Input Sector Parameters per-sector
	WO	H								
	WO	R								
	WO	N								
Result	RO	ST0								FDC formats an entire cylinder
	RO	ST1								Status information after command execution
	RO	ST2								
	RO	Undefined								
	RO	Undefined								
	RO	Undefined								
	RO	Undefined								

SCAN EQUAL									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	SK	1	0	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	STP								
Execution										Data transferred from the system to controlle6r is compared to data read from disk.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

SCAN LOW OR EQUAL									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	SK	1	1	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	STP								
Execution										Data transferred from the system to controller is compared to data read from disk.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

SCAN HIGH OR EQUAL										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	SK	1	1	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	STP								
Execution										Data transferred from the system to controller is compared to data read from disk.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

VERIFY										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	SK	1	0	1	1	0	Command Codes
	WO	EC	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL/SC								
Execution										No data transfer takes place.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

READ ID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	MFM	0	0	1	0	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
Execution										The first correct ID information on the Cylinder is stored in the Data Register.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information during execution phase
	RO	H								
	RO	R								
	RO	N								

CONFIGURE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	1	0	0	1	1	Configure Information
	WO	0	0	0	0	0	0	0	0	
	WO	0	EIS	DFIFO	POLLD	FIFOTHR				
		PRETRK								
Execution										

RE-CALIBRATE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	0	1	1	1	Command Codes
	WO	0	0	0	0	0	0	DR1	DR0	
Execution										Head retracted to Track 0

SEEK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	1	1	1	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	NCN								
Execution										Head is positioned over proper cylinder on diskette.

RELATIVE SEEK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	1	DIR	0	0	1	1	1	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	RCN								
Execution										Head is stepped in or out a programmable number of tracks.

DUMPREG									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	1	1	1	0	Command Codes
Execution										Registers placed in FIFO
Result	RO	PCN-Drive 0								
	RO	PCN-Drive 1								
	RO	PCN-Drive 2								
	RO	PCN-Drive 3								
	RO	SRT				HUT				
	RO	HLT							ND	
	RO									
	RO	LOCK	0	DC3	DC2	DC1	DC0	GAP	WG	
	RO	0	DIS	DFIFO	POLLD	FIFOTHR				
	RO	PRETRK								

LOCK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	LOCK	0	0	1	0	1	0	0	Command Codes
Result	RO	0	0	0	LOCK	0	0	0	0	

VERSION									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	1	0	0	0	0	Command Codes
Result	RO	1	0	0	1	0	0	0	0	Enhanced Controller

SENSE INTERRUPT STATUS									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	1	0	0	0	Command Codes
Result	RO	ST0								Status information at the end of each SEEK operation
	RO	PCN								

SENSE DRIVE STATUS									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	0	1	0	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
Result	RO	ST3								Status information about FDD

SPECIFY									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	0	0	1	1	Command Codes
	WO	SRT				HUT				
	WO	HLT							ND	

PERPENDICULAR MODE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	1	0	0	1	0	Command Codes
	WO	OW	0	DC3	DC2	DC1	DC0	GAP	WG	

INVALID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	Invalid codes								INVALID Command Codes (NO-OP: FDC goes into standby state)
Result	RO	ST0								ST0 = 80h